INCH-POUND

MIL-M-28787/432
17 May 1991

MILITARY SPECIFICATION

MODULES, STANDARD ELECTRONIC

MEMORY ARRAY, 128K DYNAMIC RANDOM ACCESS MODULE

KEY CODE JEJ

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the modules described herein shall consist of this specification and the latest issue of MIL-M-28787.

1. SCOPE

1.1 Scope. This document establishes the requirements and test procedures for the acquisition of an electronic memory array, 128K dynamic random access module.

1.2 Classification. This specification covers two classes of modules. Classes I and II as specified in MIL-STD-1389.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Sea Systems Command, Code SEA-55Z3, Department of the Navy, Washington, D.C. 20362-5101, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5963

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standards. The following specification and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-28787 - Modules, Standard Electronic, General Specification for.

STANDARDS

MILITARY

MIL-STD-1389 - Design Requirements for Standard Electronic Modules.

MIL-STD-1665 - Test Equipment for the Standard Electronic Modules Program.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Modules furnished under this specification shall be products which are authorized by the qualifying activity for listing on the applicable qualified products list by the time of award of contract (see 4.5).

3.2 General requirements. The module shall comply with the requirements of MIL-M-28787 except as modified herein.

3.3 Correlation requirements. Before any production modules are tested, all testers and test equipment shall be correlated in accordance with MIL-M-28787.

3.4 Failure rate requirements. All modules procured to this specification shall have a predicted failure rate no greater than 82.153 failures per million operating hours for class I or 291.674 failures per million operating hours for class II, when predicted in accordance with MIL-STD-1389. When a class II module is used in a class I environment, the failure rate for class I shall be used for reliability prediction.

3.5 Performance requirements. The module shall conform to the electrical requirements specified in table I and shall operate within the environment of design class I or class II as specified in MIL-STD-1389.

3.5.1 Substitutability. Class II modules are substitutable for class I modules. When class II modules are used in class I environments, the failure rate for class I shall be used for reliability prediction.

3.6 Module configuration requirements. The module configuration requirements shall be in accordance with MIL-STD-1389 and as specified herein.

3.6.1 Key code. The module key code shall be JEJ.

3.6.2 Size. The module size shall be 2A Format B.

3.6.3 Weight. The module shall have a maximum weight of 112 grams.

3.6.4 Contact pins. The module shall have 100 contact pins positioned 1 through 50 in one row and 51 through 100 in the other row.

3.6.5 Fin position. The module shall have an insertion and extraction and heat dissipation fin on increment A.

3.6.6 Depth. The module shall have no additional depth requirements.

TABLE I Module electrical requirements.

Test cond	Parameter 5/	Ref test table	Test type 1/-3/	25 ± 5°C 4/		Class I 4/ 0 ± 5°C 60 ± 5°C		Class II 4/ -55 ± 5°C 85 ± 5°C		Units
				Min	Max	Min	Max	Min	Max	
A1	Isolation	II	S	10	INF	10	INF	10	INF	MOhm
A2-A24	Isolation	II	X	10	INF	10	INF	10	INF	MOhm
B1-B9	Continuity	III	X	0	1	0	1	0	1	Ohm
C	Vpp stress	IV	S	----------Module shall pass all remaining tests----------						
D1-D4	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
D5-D8	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D9-D12	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
D13-D16	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D17	Ibd	V	S	0.0	0.6	0.0	0.8	0.0	0.6	µA
D18	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
D19	Ibd	V	S	0.0	0.8	0.0	0.8	0.0	0.8	µA
D20	Ibd	V	S	0.0	0.5	0.0	0.5	0.0	0.5	µA
D21-D23	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D24-D27	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
D28-D31	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D32-D35	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
D36-D39	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D40	Ibd	V	S	0.0	0.6	0.0	0.6	0.0	0.6	µA
D41	Ibd	V	S	0.0	0.5	0.0	0.5	0.0	0.5	µA
D42-D44	Ibd	V	S	0.0	0.1	0.0	0.1	0.0	0.1	µA
D45-D60	Ibd	V	S	0.0	0.2	0.0	0.2	0.0	0.2	µA
E1-E22	Ios	VI	S	-350.0	-60.0	-350.0	-60.0	-350.0	-60.0	nA
F1-F4	Ith	VII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	µA
F5-F8	Ith	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	µA
F9-F12	Ith	VII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	µA
F13-F16	Ith	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	µA
F17	Ith	VII	X	-9.6	0.12	-9.6	0.12	-9.6	0.12	µA
F18	Ith	VII	X	-3.2	0.04	-3.2	0.04	-3.2	0.04	µA
F19	Ith	VII	X	-12.8	0.16	-12.8	0.16	-12.8	0.16	µA

- See footnotes at end of table.

TABLE I. Module electrical requirements - Continued.

Test cond	Parameter 5/	Ref test table	Test type 1/-3/	25 ± 5°C 4/		Class I 4/ 0 ± 5°C 60 ± 5°C		Class II 4/ -55 ± 5°C 85 ± 5°C		Units
				Min	Max	Min	Max	Min	Max	
F20	Ilh	VII	X	-8.0	0.1	-8.0	0.1	-8.0	0.1	mA
F21-F23	Ilh	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
F24-F27	Ilh	VII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
F28-F31	Ilh	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
F32-F35	Ilh	VII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
F36-F39	Ilh	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
F40	Ilh	VII	X	-9.6	0.12	-9.6	0.12	-9.6	0.12	mA
F41	Ilh	VII	X	-8.0	0.1	-8.0	0.1	-8.0	0.1	mA
F42-F44	Ilh	VII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
F45-F60	Ilh	VII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
G1-G4	Iil	VIII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
G5-G8	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G9-G12	Iil	VIII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
G13-G16	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G17	Iil	VIII	X	-9.6	0.12	-9.6	0.12	-9.6	0.12	mA
G18	Iil	VIII	X	-3.2	0.04	-3.2	0.04	-3.2	0.04	mA
G19	Iil	VIII	X	-12.8	0.16	-12.8	0.16	-12.8	0.16	mA
G20	Iil	VIII	X	-8.0	0.1	-8.0	0.1	-8.0	0.1	mA
G21-G23	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G24-G27	Iil	VIII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
G28-G31	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G32-G35	Iil	VIII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
G36-G39	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G40	Iil	VIII	X	-9.6	0.12	-9.6	0.12	-9.6	0.12	mA
G41	Iil	VIII	X	-8.0	0.1	-8.0	0.1	-8.0	0.1	mA
G42-G44	Iil	VIII	X	-1.6	0.02	-1.6	0.02	-1.6	0.02	mA
G45-G60	Iil	VIII	X	-1.2	0.04	-1.2	0.04	-1.2	0.04	mA
H1-H22	Voh	IX	X	2.4	4.5	2.4	4.5	2.4	4.5	V
J1-J25	Vol	X	X	0.0	0.5	0.0	0.5	0.0	0.5	V
K1-K3	Iozh	XI	X	-0.05	0.05	-0.05	0.05	-0.05	0.05	mA

- See footnotes at end of table.

TABLE I. Module electrical requirements - Continued.

Test cond	Parameter 5/	Ref test table	Test type 1/-3/	25 ± 5°C 4/		Class I 4/ 0 ± 5°C 60 ± 5°C		Class II 4/ -55 ± 5°C 85 ± 5°C		Units
				Min	Max	Min	Max	Min	Max	
K4-K6	Iozl	XI	X	-0.05	0.05	-0.05	0.05	-0.05	0.05	mA
L1-L60	Vio	XII	S	-1.2	0.0	-1.2	0.0	-1.2	0.0	V
M	PSFC	XIII	S	6.7	12.5	6.7	12.5	6.7	12.5	uF
N	Icc	XIV	X	350	1210	350	1210	350	1210	mA
P1,P2	Functional	XV	X	See table XV						
Q1,Q2	Dynamic	XVI	S	See table XVI						
Q3,Q4	Dynamic	XVI	Q	See table XVI						
R1-R8	C1/D	XVIII	Q	4	75	4	75	4	75	pF
R9	C1/D	XVIII	Q	8	100	8	100	8	100	pF
R10	C1/D	XVIII	Q	4	75	4	75	4	75	pF
R11	C1/D	XVIII	Q	10	125	10	125	10	125	pF
R12	C1/D	XVIII	Q	10	100	10	100	10	100	pF
R13-R18	C1/D	XVIII	Q	4	75	4	75	4	75	pF
R19,R20	C1/D	XVIII	Q	4	100	4	100	4	100	pF
R21-R28	C1/D	XVIII	Q	2	75	2	75	2	75	pF
R29	C1/D	XVIII	Q	6	175	6	175	6	175	pF
R30	C1/D	XVIII	Q	10	100	10	100	10	100	pF
R31-R34	C1/D	XVIII	Q	2	75	2	75	2	75	pF
R35	C1/D	XVIII	Q	2	100	2	100	2	100	pF
R36,R37	C1/D	XVIII	Q	2	75	2	75	2	75	pF
R38	C1/D	XVIII	Q	2	100	2	100	2	100	pF
R39-R60	C1/D	XVIII	Q	4	75	4	75	4	75	pF
T	PSTR	XIX	Q	0	400	0	400	0	400	mV

- See footnotes on next page.

1/ "X" parameters shall be 100 percent tested during the module acceptance test.

2/ "S" parameters shall be sample acceptance tested (1 percent or two modules from each inspection lot, whichever is greater) at 25°C.

3/ "Q" parameters shall be tested during qualification testing only.

4/ Unless otherwise specified in the test table, limits are for initial and end-of-life.

5/ Abbreviations used in table I are defined in 6.1.

3.6.7 Holddown holes. The module shall have no additional requirements for location or quantity of holddown holes.

3.6.8 Marking. Marking shall be as specified in MIL-STD-1389, and the module shall be marked with the military part or identifying number M28787/432-1 for class I and M28787/432-2 for class II. No marking shall interfere with heat dissipation from the fin (such as affixing a label which may act as a heat barrier).

3.7 Circuit pin configuration. The functional block diagram shall conform to figure 1. The pin assignments shall conform to figure 2.

3.8 Acceptance test. All production modules shall be tested in accordance with footnotes 1 and 2 in table I.

3.9 End-of-life limits. Modules which have been plugged into an operating system, or exceed 2 years from date of manufacture and are to be tested, shall be capable of conforming to the 25°C end-of-life limits in table I (see 6.2).

3.10 Power supply voltage. Unless otherwise specified herein, the module shall be capable of conforming to the requirements in table I for a power supply voltage (Vcc) of 5.5 V dc.

3.11 Parallel outputs. Paralleling of outputs is not permissible.

4. QUALITY ASSURANCE PROVISIONS

4.1 Quality assurance. The quality assurance provisions of MIL-M-28787 shall apply.

4.2 Acceptance tests. Acceptance tests of all modules shall be in accordance with procedures and equipment specified in MIL-M-28787.

4.3 Test equipment. Test equipment specified on figures and in tables with a designator shall be as specified in MIL-STD-1665. Other equipment and components shall be as specified on the figures. Unless otherwise specified herein, all resistors shall be metal film and all capacitors shall be ceramic.

4.4 Test procedures. The module shall be tested as specified in table I.

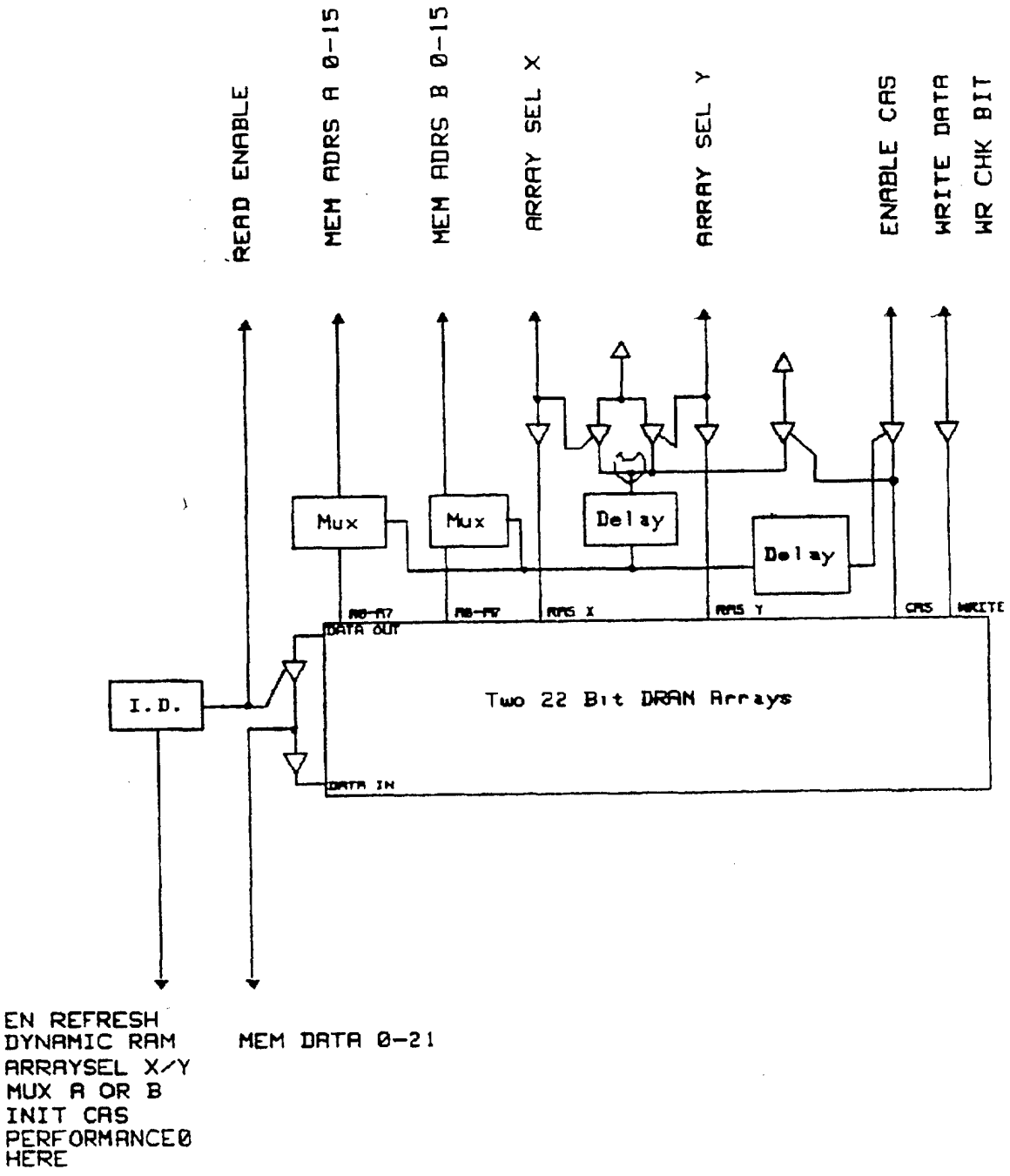


FIGURE 1. JEJ functional block diagram.

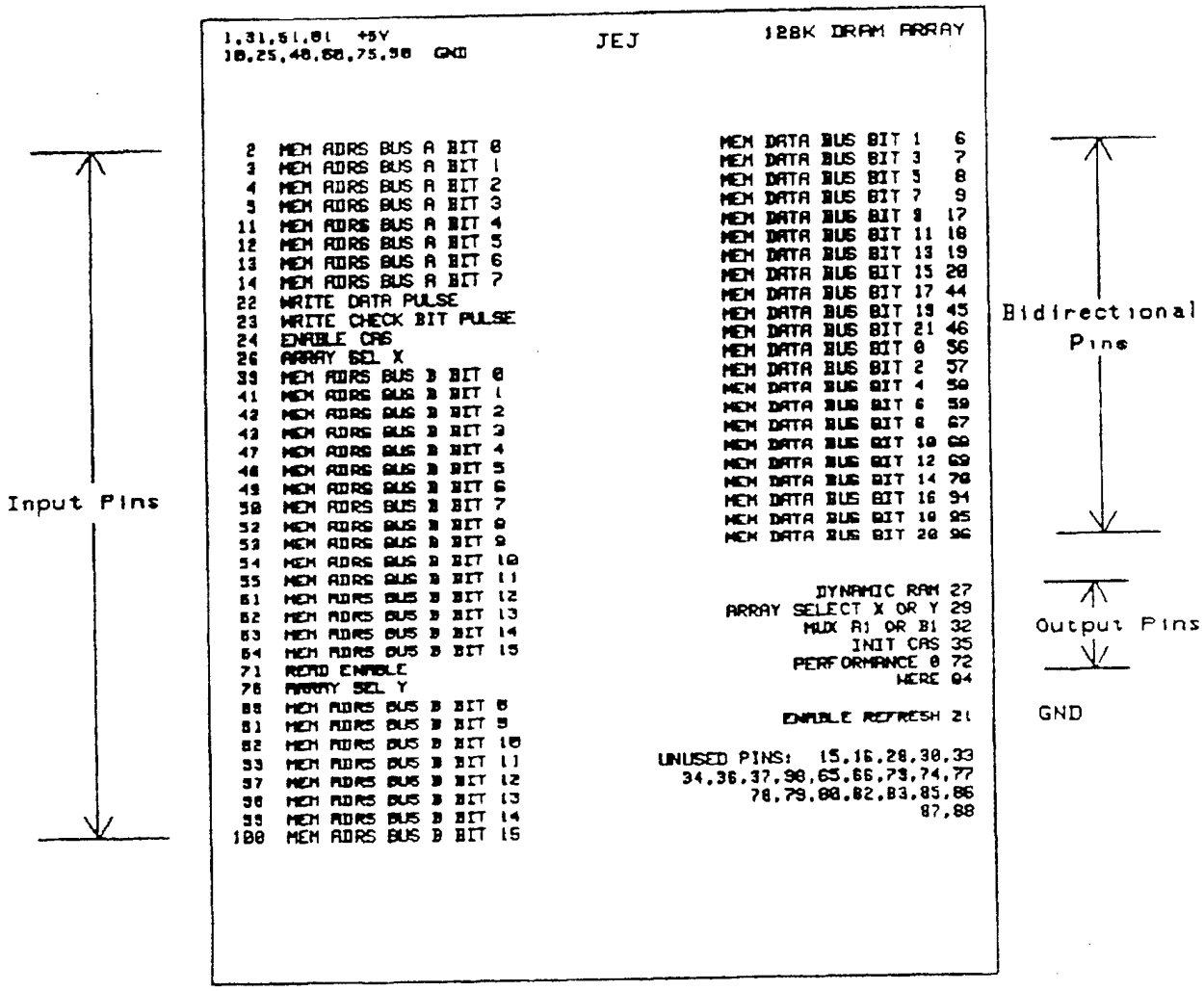


FIGURE 2. JEJ pin assignment.

4.4.1 Alternate test methods. Alternate test methods may be employed if approved by the Standard Electronic Modules Quality Assurance Activity (SEM-QAA) and they conform to the requirements of MIL-M-28787.

4.4.2 Order of testing. Test conditions A through T shall be performed in any order with the following exceptions. Test conditions A, C, D, E, and L are stress tests and shall be performed only at 25 ± 5°C. If test conditions A, C, D, E or L are part of a sequence of tests, the order of testing shall be as follows: A, C, D, E, and L where applicable, followed by the remaining tests in the sequence.

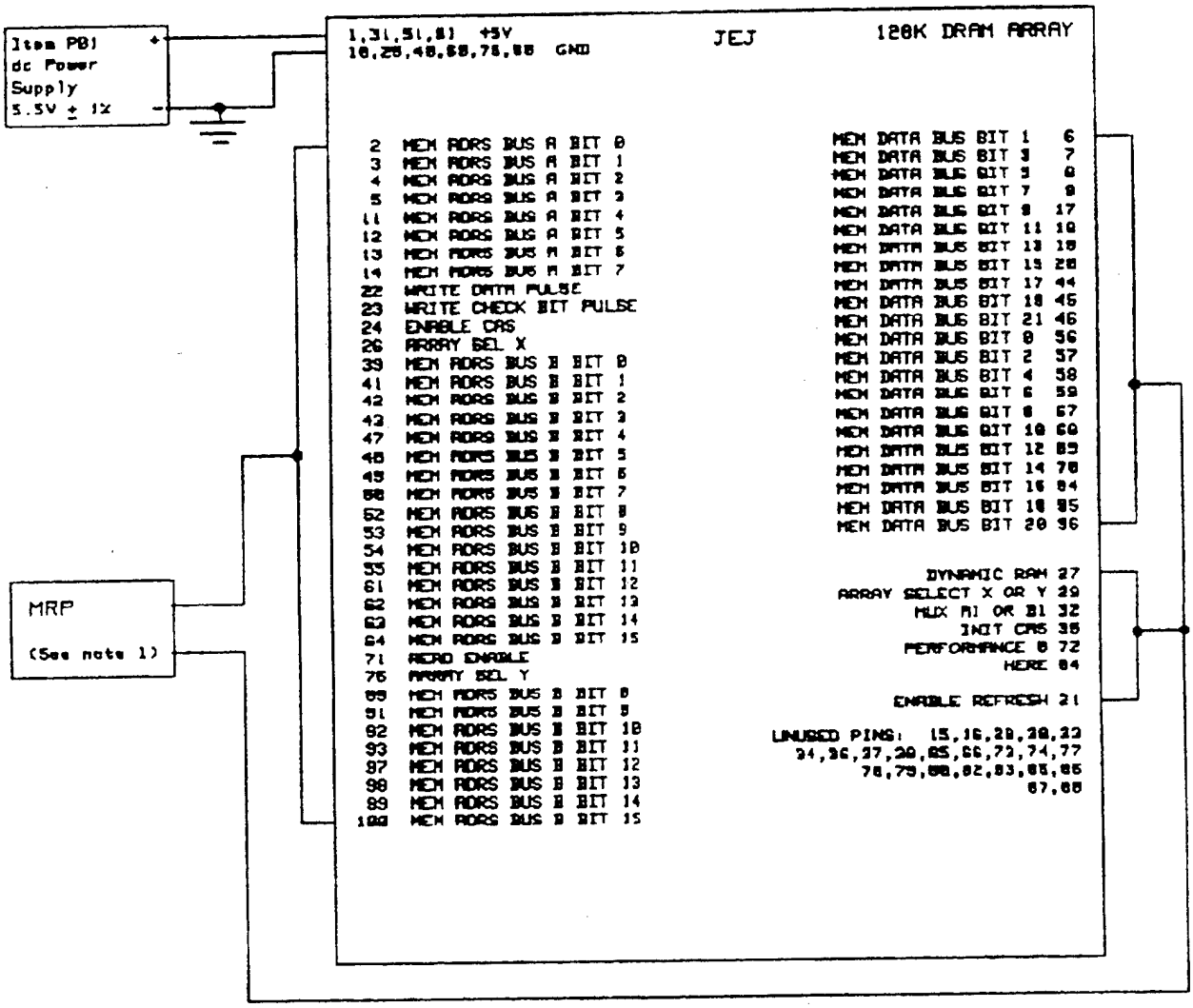
4.4.3 Multiple testing of pins. Singular pins listed multiple times in a test table indicate multiple devices connected to the pins. The module shall be tested so that each device connected to a pin is exercised and tested.

4.5 Qualification testing. Initial qualification tests and periodic check tests shall be performed in accordance with the test plan specified in MIL-M-28787 with the following modifications or additions.

4.5.1 Operating temperature tests. The operating temperature tests shall be conducted in accordance with MIL-M-28787. Before starting these tests, test conditions A through T in table I shall be performed in the order specified in 4.4.2 using the initial limits at 25°C ambient. When electrical testing is called for at the end of each temperature stabilization period, test conditions B, F through K and M through Q shall be performed in the order specified in 4.4.2 using the initial limits for the applicable operating temperature. At all other times during the operating temperature tests, the module shall be operated in the test circuit shown on figure 3.

4.5.1.1 Component temperature test. The component temperature test shall be conducted in accordance with MIL-M-28787. The module shall be operated as shown on figure 3.

4.5.2 Vibration tests. The vibration tests shall be conducted in accordance with MIL-M-28787. During the vibration tests, the module shall be operated in the test circuit shown on figure 4. Following the vibration tests, the electrical tests in table I which are marked with an "X" in the test type column, and test condition M, shall be performed using the initial limits at 25 ± 5°C ambient.



NOTE:

1. Military Reconfigurable Processor (MRP) or emulator capable of reproducing system backpanel characteristics.

FIGURE 3. JEJ operating temperature and component temperature test circuit.

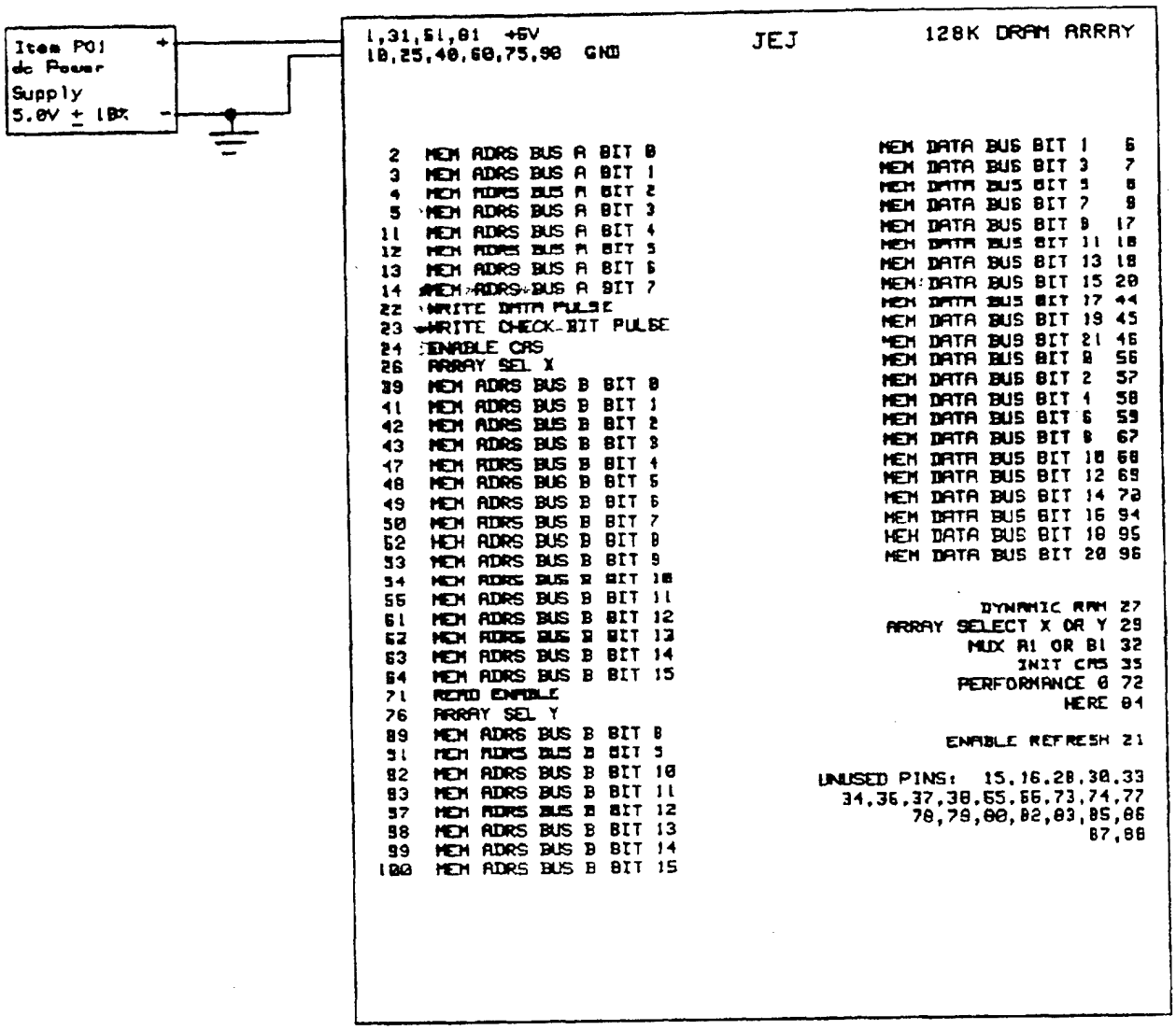


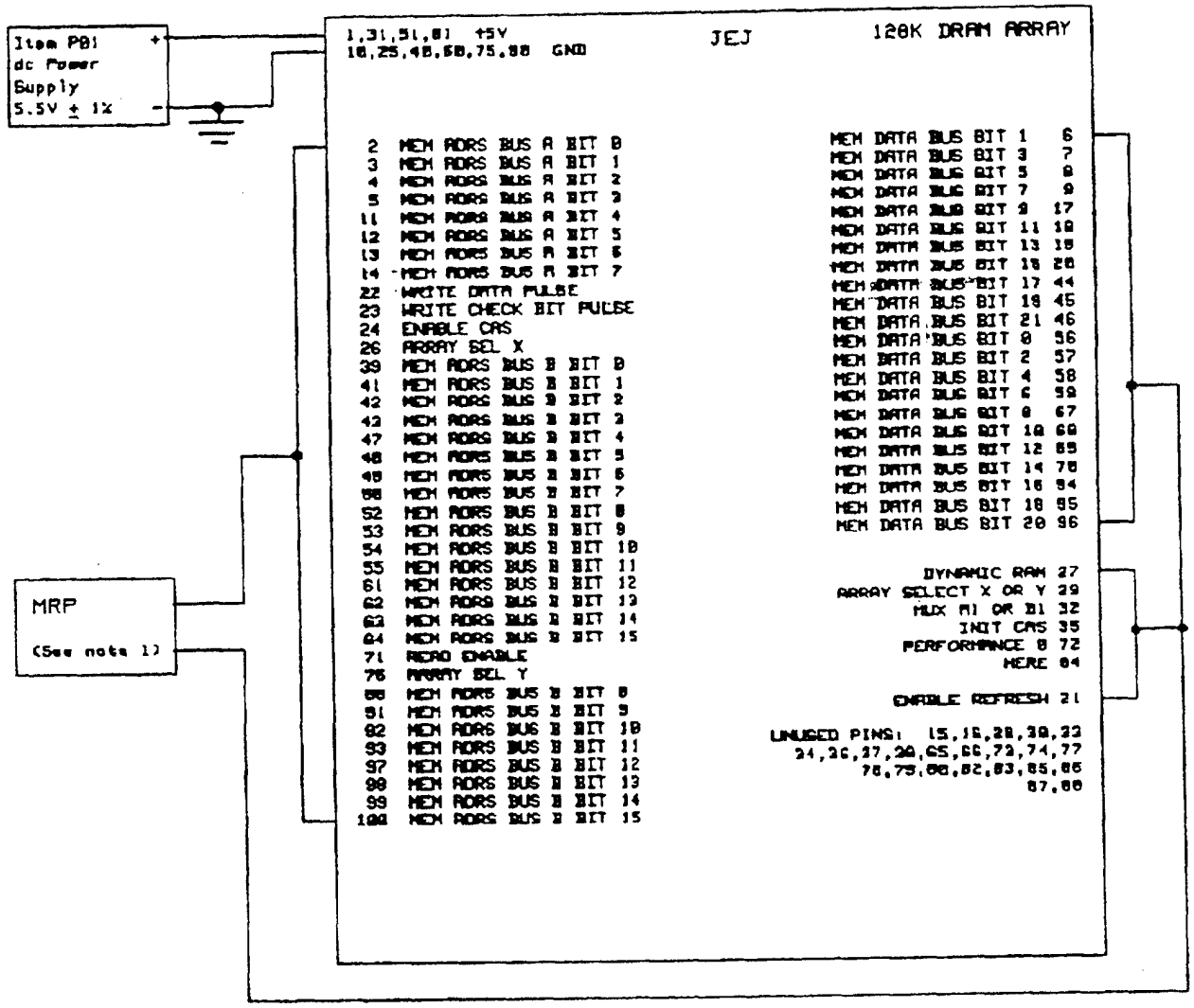
FIGURE 4. JEJ vibration test circuit.

4.5.3 Life test. The life test shall be conducted in accordance with MIL-M-28787. The module shall be operated as shown on figure 5. Following the life test and while still at the maximum class temperature, electrical tests B, F through K and M through Q shall be performed in the order specified in 4.4.2 using the operating temperature end-of-life requirements in table I. Following the return of the module to 25 ± 5°C, electrical tests B, F through K and M through Q shall be performed in the order specified in 4.4.2 using the 25 ± 5°C ambient end-of-life requirements in table I.

4.5.4 Thermal shock test. The thermal shock test shall be conducted in accordance with MIL-M-28787. The module shall be unpowered during this test. Following the thermal shock test, the electrical tests in table I which are marked with an "X" in the test type column, shall be performed using the initial limits at 25 ± 5°C ambient.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-28787.



NOTE:

1. MRP or emulator capable of reproducing system backpanel characteristics.

FIGURE 5. JEJ life test circuit.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Definitions. Negative (-) current is current directed out of the module pin and positive (+) current is current directed into the module pin. Abbreviations used in this specification are defined as follows:

(a) Cin = input capacitance.
(b) Ci/o = input/output capacitance.
(c) Cout = output capacitance.
(d) Ibd = input breakdown current.
(e) Icc = power supply current.
(f) Iih = input high level current.
(g) Iil = input low level current.
(h) Iin = input forcing current.
(i) Ioh = output high level current.
(j) Iol = output low level current.
(k) Ios = output short circuit current.
(l) Iozh = output high level leakage current.
(m) Iozl = output low level leakage current.
(n) NA = not applicable.
(o) PSFC = power supply filter capacitance.
(p) PSTA = power supply transient amplitude.
(q) Vic = input clamp diode voltage.
(r) Vih = input high level voltage.
(s) Vil = input low level voltage.
(t) Vin = input forcing voltage.
(u) Voh = output high level voltage.
(v) Vol = output low level voltage.
(w) Vout = output forcing voltage.

6.2 End-of-life. When any individual module circuit parameter fails to conform to the end-of-life requirements in table I, the module is considered to have completed its useful life (see 3.9).

6.3 Module description. The following electrical parameters reflect the -55°C to 85°C end-of-life parameters in table I. Operating power supply voltage range: 4.5 V dc to 5.5 V dc. Module power dissipation: 6.66 W (max); 3.46 W (typical).

6.3.1 Input parameters.

Signal	Vic min (V)	Vil max (V)	Vih min (V)	Iil min (mA)	Iih max (mA)	Ibd max (mA)	Cin max (pF)
MEM ADRS A 0	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 1	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 2	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 3	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 4	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 5	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 6	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 7	-1.2	0.4	2.4	-1.2	0.04	0.2	75
WRITE DATA	-1.2	0.4	2.4	-9.6	0.12	0.6	100
WR CHK BIT	-1.2	0.4	2.4	-3.2	0.04	0.2	75
ENABLE CAS	-1.2	0.4	2.4	-12.8	0.16	0.8	125
ARRAY SEL X	-1.2	0.4	2.4	-8.0	0.1	0.5	100
MEM ADRS B 0	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 1	-1.2	0.4	2.4	-1.2	0.04	0.2	75

6.3.1 Input parameters - Continued.

Signal	Vic min (V)	Vil max (V)	Vih min (V)	Iil min (mA)	Iih max (mA)	Ibd max (mA)	Cin max (pF)
MEM ADRS B 2	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 3	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 4	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 5	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 6	-1.2	0.4	2.4	-1.2	0.04	0.2	100
MEM ADRS B 7	-1.2	0.4	2.4	-1.2	0.04	0.2	100
MEM ADRS A 8	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A 9	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A10	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A11	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A12	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A13	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A14	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS A15	-1.2	0.4	2.4	-1.2	0.04	0.2	75

6.3.1 Input parameters - Continued.

Signal	Vic min (V)	Vil max (V)	Vih min (V)	Iil min (mA)	Iih max (mA)	Ibd max (mA)	Cin max (pF)
READ ENABLE	NA	0.4	2.4	-9.6	0.12	0.6	175
ARRAY SEL Y	-1.2	0.4	2.4	-8.0	0.1	0.5	100
MEM ADRS B 8	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B 9	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B10	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B11	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B12	-1.2	0.4	2.4	-1.2	0.04	0.2	100
MEM ADRS B13	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEMA DRS B14	-1.2	0.4	2.4	-1.2	0.04	0.2	75
MEM ADRS B15	-1.2	0.4	2.4	-1.2	0.04	0.2	100
MEM DATA 1	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 3	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 5	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 7	-1.2	0.4	2.4	-1.6	0.02	0.1	75

6.3.1 Input parameters - Continued.

Signal	Vic min (V)	Vil max (V)	Vih min (V)	Iil min (mA)	Iih max (mA)	Ibd max (mA)	Cin max (pF)
MEM DATA 9	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 11	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 13	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 15	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 17	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 19	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 21	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 0	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 2	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 4	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 6	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 8	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 10	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 12	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 14	-1.2	0.4	2.4	-1.6	0.02	0.1	75

6.3.1 Input parameters - Continued.

Signal	Vic min (V)	Vil max (V)	Vih min (V)	Iil min (mA)	Iih max (mA)	Ibd max (mA)	Cin max (pF)
MEM DATA 16	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 18	-1.2	0.4	2.4	-1.6	0.02	0.1	75
MEM DATA 20	-1.2	0.4	2.4	-1.6	0.02	0.1	75

6.3.2 Output parameters.

Signal	Voh min (V)	Vol max (V)	Ioh max (mA)	Iol max (mA)	Iozh max (mA)	Iozl max (mA)	Ios max (mA)	Cout max (pF)
DYNAMIC RAM	NA	0.5	-0.4	6.0	0.05	0.05	NA	NA
ARRAYSEL X/Y	NA	NA	NA	NA	NA	NA	NA	NA
MUX A OR B	NA	NA	NA	NA	NA	NA	NA	NA
INIT CAS	NA	NA	NA	NA	NA	NA	NA	NA
PERFORMANCE0	NA	0.5	-0.4	6.0	0.05	0.05	NA	NA
HERE	NA	0.5	-0.4	6.0	0.05	0.05	NA	NA
MEM DATA 1	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 3	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 5	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 7	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 9	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 11	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 13	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 15	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75

6.3.2 Output parameters - Continued.

Signal	Voh min (V)	Vol max (V)	Ioh max (mA)	Iol max (mA)	Iozh max (mA)	Iozl max (mA)	Ios max (mA)	Cout max (pF)
MEM DATA 17	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 19	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 21	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 0	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 2	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 4	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 6	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 8	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 10	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 12	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 14	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 16	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 18	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75
MEM DATA 20	2.4	0.5	-0.4	6.0	NA	NA	-60.0	75

6.3.3 Class I and II dynamic parameters.

Ref num	Sym	Parameter	Minimum limit			Maximum limit			Unit	Figs
			-55°C	25°C	85°C	-55°C	25°C	85°C		
1	tsu	MEM ADRS A 0-15 to ARRAY SEL X	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS A 0-15 to ARRAY SEL Y	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS B 0-15 to ARRAY SEL X	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS B 0-15 to ARRAY SEL Y	10	10	10	-	-	-	nS	12
2	tsu	ARRAY SEL X to ENABLE CAS	27	27	27	-	-	-	nS	12
2	tsu	ARRAY SEL Y to ENABLE CAS	27	27	27	-	-	-	nS	12
3	tsu	ARRAY SEL X to READ ENABLE	85	85	85	-	-	-	nS	12
3	tsu	ARRAY SEL Y to READ ENABLE	85	85	85	-	-	-	nS	12
4	tpd	ARRAY SEL X to MEM DATA 0-21	-	-	-	180	180	180	nS	12
4	tpd	ARRAY SEL Y to MEM DATA 0-21	-	-	-	180	180	180	nS	12

6.3.3 Class I and II dynamic parameters - Continued.

Ref num	Sym	Parameter	Minimum limit			Maximum limit			Unit	Figs
			-55°C	25°C	85°C	-55°C	25°C	85°C		
5	tsu	READ ENABLE to ENABLE CAS	1	1	1	-	-	-	nS	12
6	tsu	READ ENABLE to MEM ADRS A 0-15	0	0	0	-	-	-	nS	12
6	tsu	READ ENABLE to MEM ADRS B 0-15	0	0	0	-	-	-	nS	12
7	tpw	ARRAY SEL X	156	156	156	-	-	-	nS	12
7	tpw	ARRAY SEL Y	156	156	156	-	-	-	nS	12
8	tsu	ARRAY SEL X to WRITE DATA	83	83	83	-	-	-	nS	12
8	tsu	ARRAY SEL Y to WRITE DATA	83	83	83	-	-	-	nS	12
9	tsu	MEM DATA 0-21 to WRITE DATA	9	9	9	-	-	-	nS	12
10	tpw	WRITE DATA	50	50	50	-	-	-	nS	12
11	tsu	WRITE DATA to MEM ADRS A 0-15	8	8	8	-	-	-	nS	12
11	tsu	WRITE DATA to MEM ADRS B 0-15	8	8	8	-	-	-	nS	12

6.4 Module function. The Dynamic Random Access Memory (DRAM) array module contains two arrays of DRAM called array X and array Y, with each array containing 65,536 22-bit memory locations. DRAMs are organized on the memory array module such that array X and array Y each contain 22 DRAMs. Each of the DRAM Integrated Circuits (ICs) contain 65,536 one-bit memory locations corresponding to one bit of the data word. Data receivers get data from the memory data bus and drive the DRAM data input. Data drivers receive data from the DRAM and drive the memory data bus. The control signal receivers/buffers corresponding to one of the two 64K arrays are enabled when a reference is made to one of the on-module arrays. Each of the 44 DRAM ICs has eight address bit inputs, one data bit input and one data bit output. The address bit inputs are time multiplexed with two separate 8-bit address fields (called row address and column address) that are strobed at the beginning of each memory cycle by two clocks, Column Address Strobe (CAS) and Row Address Strobe (RAS), from the memory control module. Memory address bus bits 15-8 contain the row address; memory address bus bits 7-0 contain the column address. Memory address bits 21-16 are used for array selection. RAS corresponds to one of the 16 array select signals which specify one of the X or Y arrays. CAS is enabled to all of the memory array modules but is only recognized on the array module previously selected by the array select signals. Write enables for the DRAMs are generated by the memory timing module from common bus function bits. The DRAM arrays are divided into even data bits and odd data bits to conform to module logic partitioning. The address lines to each array are time multiplexed at the beginning of each memory cycle by the RAS and the CAS. A total of 16 address bits decode one of 65,536 single-bit cell locations within the DRAM IC. One of 16 memory arrays within the entire memory system is selected by one of eight array select X or array select Y signals from the memory control module. The memory control module generates eight array select X and eight array select Y signals from common bus address bits 19-16. Array select X and Y signals are used on the memory array module to generate the RAS. CAS enable is generated on the memory control module from the latch address signal and is in synchronization with the timing sequence selected by the cycle in progress. Write enables for the DRAMs are generated by the memory timing module from common bus function bits. Write enables for bits 21-16 are generated and driven separately by the memory timing module to allow for the disable Error Detection and Correction (EDC) function.

6.4.1 Refresh. Data bits in the DRAM are held by capacitor charge, which decays with time and temperature. The DRAM data is refreshed once every 2 milliseconds in order to

retain the correct state of the memory cell. Refresh is performed by cycling through 128 row address locations. A read or write automatically refreshes the bits associated with the referenced row.

6.4.2 A1/A2/B1/B2 multiplexer. The eight A/B multiplexers are used to perform time multiplexing of the address bits during a memory cycle. Selection is controlled by delay of the array select X/Y signals (RAS) from the memory control module. Multiplexer outputs target the following DRAMs (all are for array X and Y unless specifically noted, i.e., Y11 is array Y, bit 11 only):

(a) A1 Mux = DRAMs 1, 3, 5, 7, 9, Y11.
(b) A2 Mux = DRAMs 0, 2, 4, 6, 8, Y10.
(c) B1 Mux = DRAMs X11, 13, 15, 17, 19, 21.
(d) B2 Mux = DRAMs X10, 12, 14, 16, 18, 20.

6.4.3 Data out drivers. The data out drivers are 3-state, inverted output circuits for driving the memory data lines. The enable for the drivers is one of the eight unique read enable signals generated from the common bus function bits on the memory timing module.

6.4.4 Data in receivers. The data in receivers are 3-state, inverted circuits which receive data from the memory data lines and drive the DRAM data input(s). These receivers are constantly enabled.

6.4.5 Control receivers. The control receivers are 3-state, circuits which receive control signals from memory timing and memory control modules (i.e., RAS, enable CAS, init write data, etc.) and drive the DRAM control inputs.

6.4.6 Delay lines. Delay lines 1 and 2 provide the proper timing relationship between RAS, A/B address multiplexer switching and CAS enabling. Delay line 1 delays RAS by 10 nanoseconds. This allows the row address (memory address A/B lines 15-8) time time to be driven through the A/B multiplexers and latched into the DRAM by the already active RAS. The output of delay line 1 is the mux A1 or B1 signal and mux A2 and B2 signals which become active to select memory address lines 7-0 (column address) at the A/B multiplexers. These signals are delayed by delay line 2 delayed by delay line 2 (15 nanoseconds) to provide CAS selection at the control receivers. CAS is applied to the DRAM to latch the already active column address.

6.4.7 Memory array miscellaneous strapped signals. The memory array modules must be strapped in the backpanel to identify the size, type, speed and presence of an installed

memory array. These signals are:

(a) Size 1-0.
(b) Type 1-0.
(c) Performance 0.
(d) Here.

6.4.8 Description of I/O pins.

Signal name	Pin number	I/O	Description
MEM ADRS A 0	2	I	MEM ADRS BUS A BIT 0
MEM ADRS A 1	3	I	MEM ADRS BUS A BIT 1
MEM ADRS A 2	4	I	MEM ADRS BUS A BIT 2
MEM ADRS A 3	5	I	MEM ADRS BUS A BIT 3
MEM ADRS A 4	11	I	MEM ADRS BUS A BIT 4
MEM ADRS A 5	12	I	MEM ADRS BUS A BIT 5
MEM ADRS A 6	13	I	MEM ADRS BUS A BIT 6
MEM ADRS A 7	14	I	MEM ADRS BUS A BIT 7
WRITE DATA	22	I	WRITE DATA PULSE
WR CHK BIT	23	I	WRITE CHECK BIT PULSE
ENABLE CAS	24	I	ENABLE CAS
ARRAY SEL X	26	I	ARRAY SEL X
MEM ADRS B 0	39	I	MEM ADRS BUS B BIT 0
MEM ADRS B 1	41	I	MEM ADRS BUS B BIT 1
MEM ADRS B 2	42	I	MEM ADRS BUS B BIT 2
MEM ADRS B 3	43	I	MEM ADRS BUS B BIT 3
MEM ADRS B 4	47	I	MEM ADRS BUS B BIT 4
MEM ADRS B 5	48	I	MEM ADRS BUS B BIT 5
MEM ADRS B 6	49	I	MEM ADRS BUS B BIT 6
MEM ADRS B 7	50	I	MEM ADRS BUS B BIT 7

6.4.8 Description of I/O pins - Continued.

Signal name	Pin number	I/O	Description
MEM ADRS A 8	52	I	MEM ADRS BUS A BIT 8
MEM ADRS A 9	53	I	MEM ADRS BUS A BIT 9
MEM ADRS A10	54	I	MEM ADRS BUS A BIT 10
MEM ADRS A11	55	I	MEM ADRS BUS A BIT 11
MEM ADRS A12	61	I	MEM ADRS BUS A BIT 12
MEM ADRS A13	62	I	MEM ADRS BUS A BIT 13
MEM ADRS A14	63	I	MEM ADRS BUS A BIT 14
MEM ADRS A15	64	I	MEM ADRS BUS A BIT 15
READ ENABLE	71	I	READ ENABLE
ARRAY SEL Y	76	I	ARRAY SEL Y
MEM ADRS B 8	89	I	MEM ADRS BUS B BIT 8
MEM ADRS B 9	91	I	MEM ADRS BUS B BIT 9
MEM ADRS B10	92	I	MEM ADRS BUS B BIT 10
MEM ADRS B11	93	I	MEM ADRS BUS B BIT 11
MEM ADRS B12	97	I	MEM ADRS BUS B BIT 12
MEM ADRS B13	98	I	MEM ADRS BUS B BIT 13
MEM ADRS B14	99	I	MEM ADRS BUS B BIT 14
MEM ADRS B15	100	I	MEM ADRS BUS B BIT 15
DYNAMIC RAM	27	O	DYNAMIC RAM
ARRAYSEL X/Y	29	O	ARRAY SELECT X OR Y

6.4.8 Description of I/O pins - Continued.

Signal name	Pin number	I/O	Description
MUX A OR B	32	O	MUX A1 OR B1
INIT CAS	35	O	INIT CAS
PERFORMANCE0	72	O	PERFORMANCE 0
HERE	84	O	HERE
MEM DATA 1	6	I/O	MEM DATA BUS BIT 1
MEM DATA 3	7	I/O	MEM DATA BUS BIT 3
MEM DATA 5	8	I/O	MEM DATA BUS BIT 5
MEM DATA 7	9	I/O	MEM DATA BUS BIT 7
MEM DATA 9	17	I/O	MEM DATA BUS BIT 9
MEM DATA 11	18	I/O	MEM DATA BUS BIT 11
MEM DATA 13	19	I/O	MEM DATA BUS BIT 13
MEM DATA 15	20	I/O	MEM DATA BUS BIT 15
MEM DATA 17	44	I/O	MEM DATA BUS BIT 17
MEM DATA 19	45	I/O	MEM DATA BUS BIT 19
MEM DATA 21	46	I/O	MEM DATA BUS BIT 21
MEM DATA 0	56	I/O	MEM DATA BUS BIT 0
MEM DATA 2	57	I/O	MEM DATA BUS BIT 2
MEM DATA 4	58	I/O	MEM DATA BUS BIT 4
MEM DATA 6	59	I/O	MEM DATA BUS BIT 6
MEM DATA 8	67	I/O	MEM DATA BUS BIT 8

6.4.8 Description of I/O pins - Continued.

Signal name	Pin number	I/O	Description
MEM DATA 10	68	I/O	MEM DATA BUS BIT 10
MEM DATA 12	69	I/O	MEM DATA BUS BIT 12
MEM DATA 14	70	I/O	MEM DATA BUS BIT 14
MEM DATA 16	94	I/O	MEM DATA BUS BIT 16
MEM DATA 18	95	I/O	MEM DATA BUS BIT 18
MEM DATA 20	96	I/O	MEM DATA BUS BIT 20

6.5 Functional test vectors. Functional test vectors are not printed herein because of their extreme length; and, even when presented as a hard copy, they require conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of inspection, a test program output should be generated in a form compatible with test system architecture (magnetic tape format usually preferred). For reference purposes, the Naval Weapons Support Center (Code 607) maintains a limited quantity of dated, hard copy printouts of the functional test vectors and these may be obtained upon request.

Custodians:
Army - ER
Navy - SH
Air Force - 85

Review activities:
Army - AT
Navy - AS, MC
Air Force - 13, 19
DLA - ES

Preparing activity:
Navy - SH

(Project 5963-0075)

Agent: NW

TABLE II. Isolation test.

Test cond	Test description	Connect A to pin	Connect B to pin	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
A1	Isolation, frame	C,15, 16,28, 30,33, 34,36, 37,38, 65,66, 73,74, 77,78, 79,80, 82,83, 85,86, 87,88	Frame	10	INF	MOhm	1-9
A2	Isolation, used to unused pins	C	15,16, 28,30, 33,34, 36,37, 38,65, 66,73, 74,77, 78,79, 80,82, 83,85, 86,87,88	10	INF	MOhm	1-9
A3-A24	Isolation, unused to unused pins	see note 4		10	INF	MOhm	1-9

NOTES:

1. Isolation test tolerance table.

Condition	Value	Accuracy	Test condition
Megohm bridge voltage	100 V	± 10 percent	A1-A24
Isolation measurement	NA	± 500 KOhm	A1-A24

2. The ohmmeter used shall be item R06.

3. In the set-up conditions in table II, 'A' shall correspond to the positive terminal of the megohm bridge, 'B' shall correspond to the negative terminal and 'C' shall correspond to all used pins shorted together.

4. The unused pins on this module are: 15,16,28,30,33,34,36, 37,38,65,66,73,74,77,78,79,80,82,83,85,86,87,88.

5. Warning: When using a megohm bridge, high voltage may be present at any of the output binding posts. Always set the megohm bridge function switch to "DISCHARGE" before connecting or disconnecting the test leads.

6. When testing for frame isolation, penetrate the anodized finish on the module frame with a sharply pointed probe connected to the negative terminal of the megohm bridge.

7. Caution: Set megohm bridge to limit current to 10 uA before applying voltage to the module.

8. The test circuit shall be as indicated on figure 6.

9. Abbreviations used are defined in 6.1.

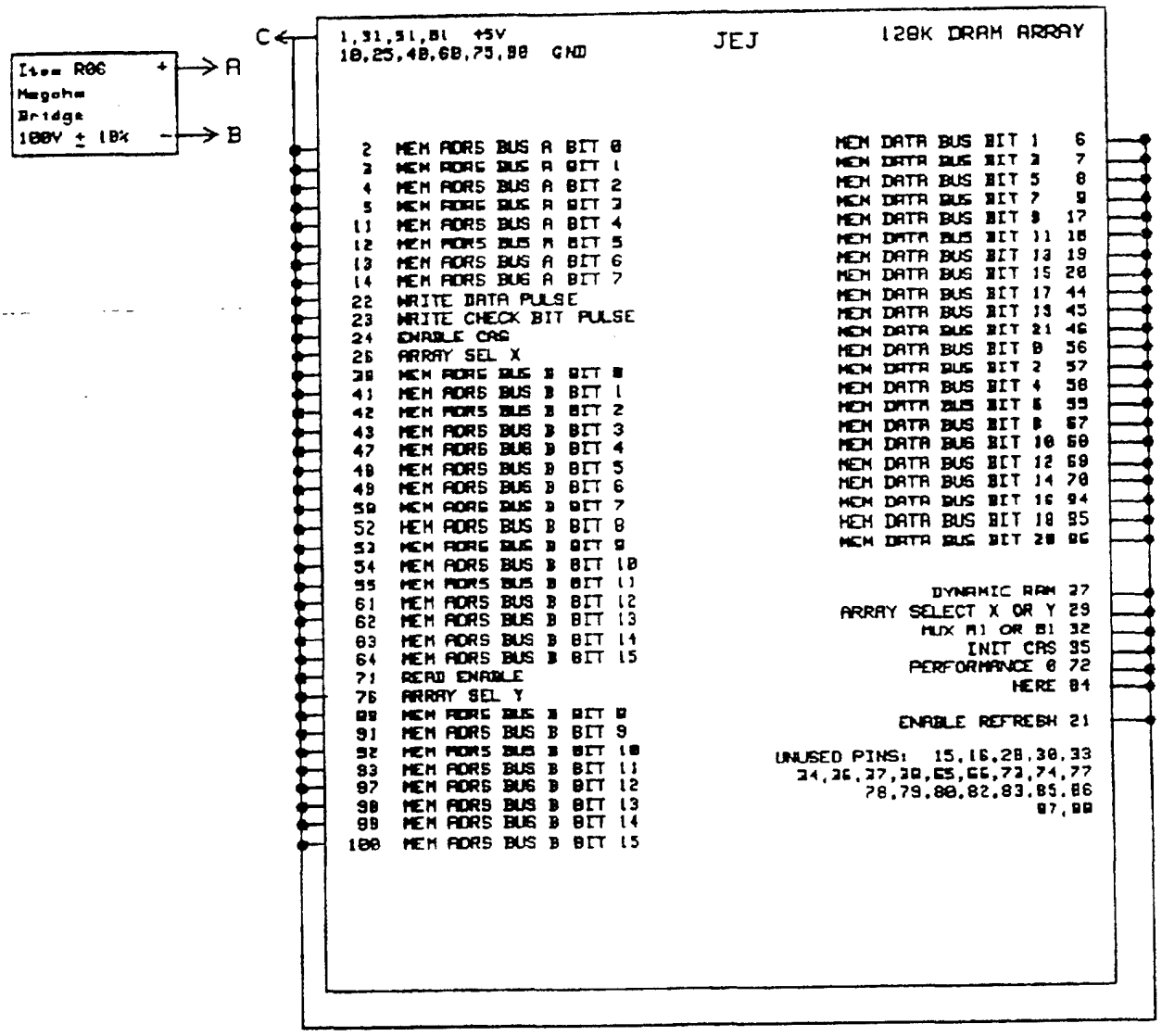


FIGURE 6. Isolation test circuit for table II.

TABLE III. Continuity test.

Test cond	Test description	Connect A to pin	Connect B to pin	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
B1	Continuity, GND	10	25	0	1	Ohm	1-5
B2	Continuity, GND	10	40				
B3	Continuity, GND	10	60				
B4	Continuity, GND	60	75				
B5	Continuity, GND	60	90				
B6	Continuity, Vcc	1	31				
B7	Continutiy, Vcc	1	51				
B8	Continuity, Vcc	51	81				
B9	Continuity, GND	10	21	0	1	Ohm	1-5

NOTES:

1. Continuity test tolerance table.

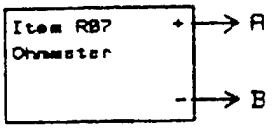
Condition	Value	Accuracy	Test condition
Continuity measurement	NA	± 0.05 Ohm	B1-B9

2. The ohmmeter used shall be item R07.

3. In the set-up conditions in table III, 'A' shall correspond to the positive terminal of the ohmmeter, and 'B' shall correspond to the negative terminal.

4. The test circuit shall be as indicated on figure 7.

5. Abbreviations used are defined in 6.1.



1,31,61,81 +5V
10,25,40,60,75,90 GND

JEJ

128K DRAM ARRAY

2	MEM ADRS BUS A BIT 0	MEM DATA BUS BIT 1	6
3	MEM ADRS BUS A BIT 1	MEM DATA BUS BIT 3	7
4	MEM ADRS BUS A BIT 2	MEM DATA BUS BIT 5	8
5	MEM ADRS BUS A BIT 3	MEM DATA BUS BIT 7	9
11	MEM ADRS BUS A BIT 4	MEM DATA BUS BIT 9	17
12	MEM ADRS BUS A BIT 5	MEM DATA BUS BIT 11	18
13	MEM ADRS BUS A BIT 6	MEM DATA BUS BIT 13	19
14	MEM ADRS BUS A BIT 7	MEM DATA BUS BIT 15	20
22	WRITE DATA PULSE	MEM DATA BUS BIT 17	44
23	WRITE CHECK BIT PULSE	MEM DATA BUS BIT 19	45
24	ENABLE CAS	MEM DATA BUS BIT 21	46
26	ARRAY SEL X	MEM DATA BUS BIT 0	56
39	MEM ADRS BUS B BIT 0	MEM DATA BUS BIT 2	57
41	MEM ADRS BUS B BIT 1	MEM DATA BUS BIT 4	58
42	MEM ADRS BUS B BIT 2	MEM DATA BUS BIT 6	59
43	MEM ADRS BUS B BIT 3	MEM DATA BUS BIT 8	67
47	MEM ADRS BUS B BIT 4	MEM DATA BUS BIT 10	68
48	MEM ADRS BUS B BIT 5	MEM DATA BUS BIT 12	69
49	MEM ADRS BUS B BIT 6	MEM DATA BUS BIT 14	70
50	MEM ADRS BUS B BIT 7	MEM DATA BUS BIT 16	94
52	MEM ADRS BUS B BIT 8	MEM DATA BUS BIT 18	95
53	MEM ADRS BUS B BIT 9	MEM DATA BUS BIT 20	96
54	MEM ADRS BUS B BIT 10		
55	MEM ADRS BUS B BIT 11	DYNAMIC RAM	27
61	MEM ADRS BUS B BIT 12	ARRAY SELECT X OR Y	29
62	MEM ADRS BUS B BIT 13	MUX A1 OR B1	32
63	MEM ADRS BUS B BIT 14	INIT CAS	35
64	MEM ADRS BUS B BIT 15	PERFORMANCE 0	72
71	READ ENABLE	HERE	84
76	ARRAY SEL Y		
89	MEM ADRS BUS B BIT 8	ENABLE REFRESH	21
91	MEM ADRS BUS B BIT 9		
92	MEM ADRS BUS B BIT 10	UNUSED PINS: 15,16,28,30,33	
93	MEM ADRS BUS B BIT 11	34,36,37,38,65,66,73,74,77	
97	MEM ADRS BUS B BIT 12	78,79,80,82,83,85,86	
98	MEM ADRS BUS B BIT 13	87,88	
99	MEM ADRS BUS B BIT 14		
100	MEM ADRS BUS B BIT 15		

FIGURE 7. Continuity test circuit for table III.

TABLE IV. Power supply stress test.

Test cond	Power supply	Vin (V)	Connect Positive lead to	Connect Negative lead to	25 ± 5°C Initial limits	Notes
C	Vcc	7.0	1,31,51, 81	10,25, 40,60, 75,90	Module shall pass all remaining tests.	1-6

NOTES:

1. Power supply stress test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	7.0 V	+0 mV,-70 mV	C
Power supply current limit	1.692 A	NA	C

2. There shall be no power supply voltage overshoot on this test.

3. Connect the power supplies to the module as indicated in table IV.

4. When performing the power supply stress test, no measurements are taken. This condition shall be maintained for a minimum of 5 seconds.

5. The test circuit shall be as indicated on figure 8.

6. Abbreviations used are defined in 6.1.

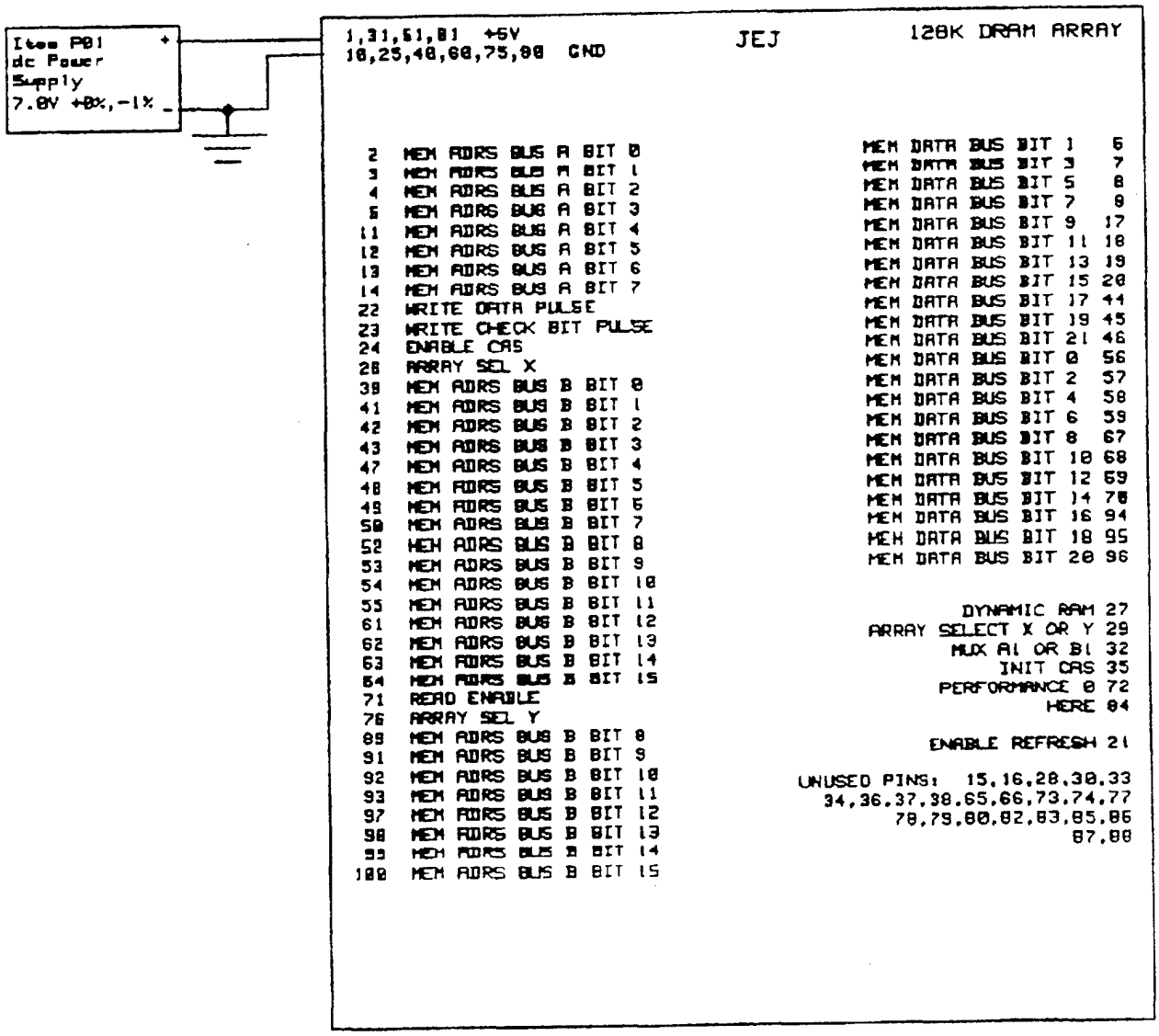


FIGURE 8. Vcc stress test circuit for table IV.

TABLE V. Input breakdown current test.

Test cond	Signal name	Pin no.	Vin (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
D1	MEM ADRS A 0	2	5.5	0.0	0.2	mA	1-3
D2	MEM ADRS A 1	3					
D3	MEM ADRS A 2	4					
D4	MEM ADRS A 3	5	5.5	0.0	0.2	mA	1-3
D5	MEM DATA 1	6	5.5	0.0	0.1	mA	1-3
D6	MEM DATA 3	7					
D7	MEM DATA 5	8					
D8	MEM DATA 7	9	5.5	0.0	0.1	mA	1-3
D9	MEM ADRS A 4	11	5.5	0.0	0.2	mA	1-3
D10	MEM ADRS A 5	12					
D11	MEM ADRS A 6	13					
D12	MEM ADRS A 7	14	5.5	0.0	0.2	mA	1-3
D13	MEM DATA 9	17	5.5	0.0	0.1	mA	1-3
D14	MEM DATA 11	18					
D15	MEM DATA 13	19					
D16	MEM DATA 15	20	5.5	0.0	0.1	mA	1-3
D17	WRITE DATA	22	5.5	0.0	0.6	mA	1-3
D18	WR CHK BIT	23	5.5	0.0	0.2	mA	1-3
D19	ENABLE CAS	24	5.5	0.0	0.8	mA	1-3
D20	ARRAY SEL X	26	5.5	0.0	0.5	mA	1-3
D21	MEM DATA 17	44	5.5	0.0	0.1	mA	1-3

TABLE V. Input breakdown current test - Continued.

Test cond	Signal name	Pin no.	Vin (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
D22	MEM DATA 19	45	5.5	0.0	0.1	mA	1-3
D23	MEM DATA 21	46	5.5	0.0	0.1	mA	1-3
D24	MEM ADRS A 8	52	5.5	0.0	0.2	mA	1-3
D25	MEM ADRS A 9	53					
D26	MEM ADRS A10	54					
D27	MEM ADRS A11	55	5.5	0.0	0.2	mA	1-3
D28	MEM DATA 0	56	5.5	0.0	0.1	mA	1-3
D29	MEM DATA 2	57					
D30	MEM DATA 4	58					
D31	MEM DATA 6	59	5.5	0.0	0.1	mA	1-3
D32	MEM ADRS A12	61	5.5	0.0	0.2	mA	1-3
D33	MEM ADRS A13	62					
D34	MEM ADRS A14	63					
D35	MEM ADRS A15	64	5.5	0.0	0.2	mA	1-3
D36	MEM DATA 8	67	5.5	0.0	0.1	mA	1-3
D37	MEM DATA 10	68					
D38	MEM DATA 12	69					
D39	MEM DATA 14	70	5.5	0.0	0.1	mA	1-3
D40	READ ENABLE	71	5.5	0.0	0.6	mA	1-3
D41	ARRAY SEL Y	76	5.5	0.0	0.5	mA	1-3
D42	MEM DATA 16	94	5.5	0.0	0.1	mA	1-3

TABLE V. Input breakdown current test - Continued.

Test cond	Signal name	Pin no.	Vin (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
D43	MEM DATA 18	95	5.5	0.0	0.1	mA	1-3
D44	MEM DATA 20	96	5.5	0.0	0.1	mA	1-3
D45	MEM ADRS B 0	39	5.5	0.0	0.2	mA	1-3
D46	MEM ADRS B 1	41					
D47	MEM ADRS B 2	42					
D48	MEM ADRS B 3	43					
D49	MEM ADRS B 4	47					
D50	MEM ADRS B 5	48					
D51	MEM ADRS B 6	49					
D52	MEM ADRS B 7	50					
D53	MEM ADRS B 8	89					
D54	MEM ADRS B 9	91					
D55	MEM ADRS B10	92					
D56	MEM ADRS B11	93					
D57	MEM ADRS B12	97					
D58	MEM ADRS B13	98					
D59	MEM ADRS B14	99					
D60	MEM ADRS B15	100	5.5	0.0	0.2	mA	1-3

NOTES:

1. Input breakdown current test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	D1-D60
Power supply current limit	1.41 A	NA	D1-D60
Forcing voltage, (Vin)	5.5 V	± 55 mV	D1-D60
Pattern voltage high, (VH) low, (VL)	 3.0 V 0.0 V	 ± 100 mV ± 100 mV	 D1-D60 D1-D60
Input current measurement	NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA	± 10 uA ± 5 uA ± 10 uA ± 5 uA ± 30 uA ± 10 uA ± 40 uA ± 25 uA ± 5 uA ± 10 uA ± 5 uA ± 10 uA ± 5 uA ± 30 uA ± 25 uA ± 5 uA ± 10 uA	D1-D4 D5,D6 D9-D12 D13-D16 D17 D18 D19 D20 D21-D23 D24-D27 D28-D31 D32-D35 D36-D39 D40 D41 D42-D44 D45-D60

NOTES: - Continued.

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing voltage shall be applied to the pin specified in the appropriate test conditions in table V and the current then measured. The forcing voltage overshoot shall not exceed 100 mV.

3. Abbreviations used are defined in 6.1.

TABLE VI. Output short circuit current test.

Test cond	Signal name	Pin no.	Vout (V)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
E1	MEM DATA 1	6	0.0	-350.0	-60.0	mA	1-4
E2	MEM DATA 3	7					
E3	MEM DATA 5	8					
E4	MEM DATA 7	9					
E5	MEM DATA 9	17					
E6	MEM DATA 0	56					
E7	MEM DATA 2	57					
E8	MEM DATA 4	58					
E9	MEM DATA 6	59					
E10	MEM DATA 8	67					
E11	MEM DATA 11	18					
E12	MEM DATA 13	19					
E13	MEM DATA 15	20					
E14	MEM DATA 17	44					
E15	MEM DATA 19	45					
E16	MEM DATA 21	46					
E17	MEM DATA 10	68					
E18	MEM DATA 12	69					
E19	MEM DATA 14	70	0.0	-350.0	-60.0	mA	1-4

TABLE VI. Output short circuit current test - Continued.

Test cond	Signal name	Pin no.	Vout (V)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
E20	MEM DATA 16	94	0.0	-350.0	-60.0	mA	1-4
E21	MEM DATA 18	95					
E22	MEM DATA 20	96	0.0	-350.0	-60.0	mA	1-4

NOTES:

1. Output short circuit current test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	E1-E22
Power supply current limit	1.41 A	NA	E1-E22
Forcing voltage, (Vout)	0.0 V	± 50 mV	E1-E22
Pattern voltage high, (VH) low, (VL)	3.0 V 0.0 V	± 100 mV ± 100 mV	E1-E22 E1-E22
Output current measurement	NA	± 14.5 mA	E1-E22

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

NOTES: - Continued.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing voltage shall be applied to the pin specified in the appropriate test conditions in table VI and the current then measured. The forcing voltage undershoot shall not exceed 100 mV.

3. When performing this test, only one output shall be tested at a time, and the duration of momentarily grounding each output shall not exceed 1 second.

4. Abbreviations used are defined in 6.1.

TABLE VII. Input current, high level, test.

Test cond	Signal name	Pin no.	Vih (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
F1	MEM ADRS A 0	2	2.4	-1.2	0.04	mA	1-3
F2	MEM ADRS A 1	3					
F3	MEM ADRS A 2	4					
F4	MEM ADRS A 3	5	2.4	-1.2	0.04	mA	1-3
F5	MEM DATA 1	6	2.4	-1.6	0.02	mA	1-3
F6	MEM DATA 3	7					
F7	MEM DATA 5	8					
F8	MEM DATA 7	9	2.4	-1.6	0.02	mA	1-3
F9	MEM ADRS A 4	11	2.4	-1.2	0.04	mA	1-3
F10	MEM ADRS A 5	12					
F11	MEM ADRS A 6	13					
F12	MEM ADRS A 7	14	2.4	-1.2	0.04	mA	1-3
F13	MEM DATA 9	17	2.4	-1.6	0.02	mA	1-3
F14	MEM DATA 11	18					
F15	MEM DATA 13	19					
F16	MEM DATA 15	20	2.4	-1.6	0.02	mA	1-3
F17	WRITE DATA	22	2.4	-9.6	0.12	mA	1-3
F18	WR CHK BIT	23	2.4	-3.2	0.04	mA	1-3
F19	ENABLE CAS	24	2.4	-12.8	0.16	mA	1-3
F20	ARRAY SEL X	26	2.4	-8.0	0.1	mA	1-3

TABLE VII. Input current, high level, test - Continued.

Test cond	Signal name	Pin no.	Vih (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
F21	MEM DATA 17	44	2.4	-1.6	0.02	mA	1-3
F22	MEM DATA 19	45					
F23	MEM DATA 21	46	2.4	-1.6	0.02	mA	1-3
F24	MEM ADRS A 8	52	2.4	-1.2	0.04	mA	1-3
F25	MEM ADRS A 9	53					
F26	MEM ADRS A10	54					
F27	MEM ADRS A11	55	2.4	-1.2	0.04	mA	1-3
F28	MEM DATA 0	56	2.4	-1.6	0.02	mA	1-3
F29	MEM DATA 2	57					
F30	MEM DATA 4	58					
F31	MEM DATA 6	59	2.4	-1.6	0.02	mA	1-3
F32	MEM ADRS A12	61	2.4	-1.2	0.04	mA	1-3
F33	MEM ADRS A13	62					
F34	MEM ADRS A14	63					
F35	MEM ADRS A15	64	2.4	-1.2	0.04	mA	1-3
F36	MEM DATA 8	67	2.4	-1.6	0.02	mA	1-3
F37	MEM DATA 10	68					
F38	MEM DATA 12	69					
F39	MEM DATA 14	70	2.4	-1.6	0.02	mA	1-3
F40	READ ENABLE	71	2.4	-9.6	0.12	mA	1-3

TABLE VII. Input current, high level, test - Continued.

Test cond	Signal name	Pin no.	Vih (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
F41	ARRAY SEL Y	76	2.4	-8.0	0.1	mA	1-3
F42	MEM DATA 16	94	2.4	-1.6	0.02	mA	1-3
F43	MEM DATA 18	95					
F44	MEM DATA 20	96	2.4	-1.6	0.02	mA	1-3
F45	MEM ADRS B 0	39	2.4	-1.2	0.04	mA	1-3
F46	MEM ADRS B 1	41					
F47	MEM ADRS B 2	42					
F48	MEM ADRS B 3	43					
F49	MEM ADRS B 4	47					
F50	MEM ADRS B 5	48					
F51	MEM ADRS B 6	49					
F52	MEM ADRS B 7	50					
F53	MEM ADRS B 8	89					
F54	MEM ADRS B 9	91					
F55	MEM ADRS B10	92					
F56	MEM ADRS B11	93					
F57	MEM ADRS B12	97					
F58	MEM ADRS B13	98					
F59	MEM ADRS B14	99					
F60	MEM ADRS B15	100	2.4	-1.2	0.04	mA	1-3

NOTES:

1. Input current, high level, test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	F1-F60
Power supply current limit	1.41 A	NA	F1-F60
Forcing voltage, (Vih)	2.4 V	± 50 mV	F1-F60
Pattern voltage high, (VH)	3.0 V	± 100 mV	F1-F60
low, (VL)	0.0 V	± 100 mV	F1-F60
Input current measurement	NA	± 62.0 uA	F1-F4
	NA	± 81.0 uA	F5-F8
	NA	± 62.0 uA	F9-F12
	NA	± 81.0 uA	F13-F16
	NA	± 490.0 uA	F17
	NA	± 162.0 uA	F18
	NA	± 650.0 uA	F19
	NA	± 410.0 uA	F20
	NA	± 81.0 uA	F21-F23
	NA	± 62.0 uA	F24-F27
	NA	± 81.0 uA	F28-F31
	NA	± 62.0 uA	F32-F35
	NA	± 81.0 uA	F36-F39
	NA	± 486.0 uA	F40
	NA	± 410.0 uA	F41
	NA	± 81.0 uA	F42-F44
	NA	± 62.0 uA	F45-F60

2. The following procedure is required to perform this test:

NOTES: - Continued.

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing voltage shall be applied to the pin specified in the appropriate test conditions in table VII and the current then measured. The forcing voltage overshoot shall not exceed 100 mV.

3. Abbreviations used are defined in 6.1.

TABLE VIII. Input current, low level, test.

Test cond	Signal name	Pin no.	Vil (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
G1	MEM ADRS A 0	2	0.4	-1.2	0.04	mA	1-3
G2	MEM ADRS A 1	3					
G3	MEM ADRS A 2	4					
G4	MEM ADRS A 3	5	0.4	-1.2	0.04	mA	1-3
G5	MEM DATA 1	6	0.4	-1.6	0.02	mA	1-3
G6	MEM DATA 3	7					
G7	MEM DATA 5	8					
G8	MEM DATA 7	9	0.4	-1.6	0.02	mA	1-3
G9	MEM ADRS A 4	11	0.4	-1.2	0.04	mA	1-3
G10	MEM ADRS A 5	12					
G11	MEM ADRS A 6	13					
G12	MEM ADRS A 7	14	0.4	-1.2	0.04	mA	1-3
G13	MEM DATA 9	17	0.4	-1.6	0.02	mA	1-3
G14	MEM DATA 11	18					
G15	MEM DATA 13	19					
G16	MEM DATA 15	20	0.4	-1.6	0.02	mA	1-3
G17	WRITE DATA	22	0.4	-9.6	0.12	mA	1-3
G18	WR CHK BIT	23	0.4	-3.2	0.04	mA	1-3
G19	ENABLE CAS	24	0.4	-12.8	0.16	mA	1-3
G20	ARRAY SEL X	26	0.4	-8.0	0.1	mA	1-3

TABLE VIII. Input current, low level, test - Continued.

Test cond	Signal name	Pin no.	Vil (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
G21	MEM DATA 17	44	0.4	-1.6	0.02	mA	1-3
G22	MEM DATA 19	45					
G23	MEM DATA 21	46	0.4	-1.6	0.02	mA	1-3
G24	MEM ADRS A 8	52	0.4	-1.2	0.04	mA	1-3
G25	MEM ADRS A 9	53					
G26	MEM ADRS A10	54					
G27	MEM ADRS A11	55	0.4	-1.2	0.04	mA	1-3
G28	MEM DATA 0	56	0.4	-1.6	0.02	mA	1-3
G29	MEM DATA 2	57					
G30	MEM DATA 4	58					
G31	MEM DATA 6	59	0.4	-1.6	0.02	mA	1-3
G32	MEM ADRS A12	61	0.4	-1.2	0.04	mA	1-3
G33	MEM ADRS A13	62					
G34	MEM ADRS A14	63					
G35	MEM ADRS A15	64	0.4	-1.2	0.04	mA	1-3
G36	MEM DATA 8	67	0.4	-1.6	0.02	mA	1-3
G37	MEM DATA 10	68					
G38	MEM DATA 12	69					
G39	MEM DATA 14	70	0.4	-1.6	0.02	mA	1-3
G40	READ ENABLE	71	0.4	-9.6	0.12	mA	1-3

TABLE VIII. Input current, low level, test - Continued.

Test cond	Signal name	Pin no.	Vil (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
G41	ARRAY SEL Y	76	0.4	-8.0	0.1	mA	1-3
G42	MEM DATA 16	94	0.4	-1.6	0.02	mA	1-3
G43	MEM DATA 18	95					
G44	MEM DATA 20	96	0.4	-1.6	0.02	mA	1-3
G45	MEM ADRS B 0	39	0.4	-1.2	0.04	mA	1-3
G46	MEM ADRS B 1	41					
G47	MEM ADRS B 2	42					
G48	MEM ADRS B 3	43					
G49	MEM ADRS B 4	47					
G50	MEM ADRS B 5	48					
G51	MEM ADRS B 6	49					
G52	MEM ADRS B 7	50					
G53	MEM ADRS B 8	89					
G54	MEM ADRS B 9	91					
G55	MEM ADRS B10	92					
G56	MEM ADRS B11	93					
G57	MEM ADRS B12	97					
G58	MEM ADRS B13	98					
G59	MEM ADRS B14	99					
G60	MEM ADRS B15	100	0.4	-1.2	0.04	mA	1-3

NOTES:

1. Input current, low level, test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	G1-G60
Power supply current limit	1.41 A	NA	G1-G60
Forcing voltage, (Vil)	0.4 V	± 50 mV	G1-G60
Pattern voltage high, (VH)	3.0 V	± 100 mV	G1-G60
low, (VL)	0.0 V	± 100 mV	G1-G60
Input current measurement	NA	± 62.0 uA	G1-G4
	NA	± 81.0 uA	G5-G8
	NA	± 62.0 uA	G9-G12
	NA	± 81.0 uA	G13-G16
	NA	± 490.0 uA	G17
	NA	± 162.0 uA	G18
	NA	± 650.0 uA	G19
	NA	± 410.0 uA	G20
	NA	± 81.0 uA	G21-G23
	NA	± 62.0 uA	G24-G27
	NA	± 81.0 uA	G28-G31
	NA	± 62.0 uA	G32-G35
	NA	± 81.0 uA	G36-G39
	NA	± 486.0 uA	G40
	NA	± 410.0 uA	G41
	NA	± 81.0 uA	G42-G44
	NA	± 62.0 uA	G45-G60

2. The following procedure is required to perform this test:

NOTES: - Continued.

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing voltage shall be applied to the pin specified in the appropriate test conditions in table VIII and the current then measured. The forcing voltage overshoot shall not exceed 100 mV.

3. Abbreviations used are defined in 6.1.

TABLE IX. Output voltage, high level, test.

Test cond	Signal name	Pin no.	Ioh (mA)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
H1	MEM DATA 1	6	-0.4	2.4	4.5	V	1-4
H2	MEM DATA 3	7					
H3	MEM DATA 5	8					
H4	MEM DATA 7	9					
H5	MEM DATA 9	17					
H6	MEM DATA 0	56					
H7	MEM DATA 2	57					
H8	MEM DATA 4	58					
H9	MEM DATA 6	59					
H10	MEM DATA 8	67					
H11	MEM DATA 11	18					
H12	MEM DATA 13	19					
H13	MEM DATA 15	20					
H14	MEM DATA 17	44					
H15	MEM DATA 19	45					
H16	MEM DATA 21	46					
H17	MEM DATA 10	68					
H18	MEM DATA 12	69					
H19	MEM DATA 14	70	-0.4	2.4	4.5	V	1-4

TABLE IX. Output voltage, high level, test - Continued.

Test cond	Signal name	Pin no.	Ioh (mA)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
H20	MEM DATA 16	94	-0.4	2.4	4.5	V	1-4
H21	MEM DATA 18	95	↓	↓	↓	↓	↓
H22	MEM DATA 20	96	-0.4	2.4	4.5	V	1-4

NOTES:

1. Output voltage, high level, test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	4.5 V	± 45 mV	H1-H22
Power supply current limit	1.41 A	NA	H1-H22
Forcing current, (Ioh)	-0.4 mA	± 40 uA	H1-H22
Pattern voltage high, (VH) low, (VL)	3.0 V 0.0 V	± 100 mV ± 100 mV	H1-H22 H1-H22
Output voltage measurement	NA	± 105 mV	H1-H22

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

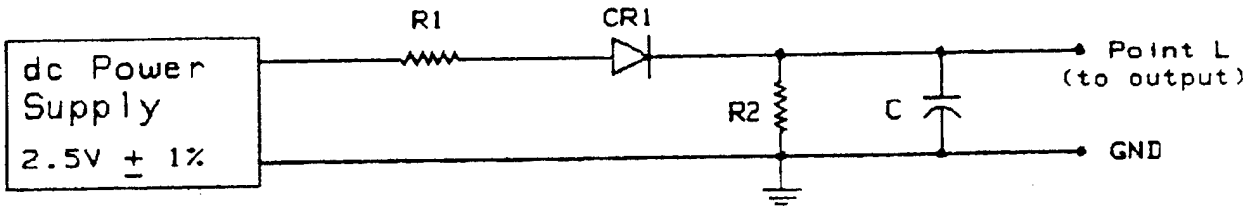
NOTES: - Continued.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing current shall be applied to the pin specified in the appropriate test conditions in table IX and the voltage then measured.

3. The load shall be as indicated on figure 9.

4. Abbreviations used are defined in 6.1.



NOTES:

1. CR1 = 1N4148 or equivalent.

2. The load capacitance is defined as follows:

(a) C = 100 ± 10 pF (including probe and parasitic capacitance) for sample dynamic tests.

(b) C = 300 ± 30 pF (including probe and parasitic capacitance) for qualification dynamic tests.

(c) The functional test shall be performed with only a 100 ± 10 pF load (including probe and parasitic capacitance) attached to each output.

(d) C not required for any other tests.

FIGURE 9. Logic load circuit.

NOTES: - Continued.

3. Select R1 for a current flow of Iol when point L is held at Vol. The values of Iol and Vol for each output are in the table below.

4. The value of R2 for each output load shall be as specified in the table below.

Pin number	R2 1/ (ohms)	Iol (mA)	Vol (volts)
6,7,8,9,17,18,19, 20,44,45,46,56, 57,58,59,67,68, 69,70,94,95,96	6200	6.0	0.5
27,72,84	NA	6.0	0.5

1/ All resistors are metal film, ± 1 percent, 1/4 W.

TABLE X. Output voltage, low level, test.

Test cond	Signal name	Pin no.	Iol (mA)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
J1	MEM DATA 1	6	6.0	0.0	0.5	V	1-4
J2	MEM DATA 3	7					
J3	MEM DATA 5	8					
J4	MEM DATA 7	9					
J5	MEM DATA 9	17					
J6	MEM DATA 0	56					
J7	MEM DATA 2	57					
J8	MEM DATA 4	58					
J9	MEM DATA 6	59					
J10	MEM DATA 8	67					
J11	DYNAMIC RAM	27					
J12	PERFORMANCE0	72					
J13	HERE	84					
J14	MEM DATA 11	18					
J15	MEM DATA 13	19					
J16	MEM DATA 15	20					
J17	MEM DATA 17	44					
J18	MEM DATA 19	45					
J19	MEM DATA 21	46					
J20	MEM DATA 10	68	6.0	0.0	0.5	V	1-4

TABLE X. Output voltage, low level, test - Continued.

Test cond	Signal name	Pin no.	Iol (mA)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
J21	MEM DATA 12	69	6.0	0.0	0.5	V	1-4
J22	MEM DATA 14	70					
J23	MEM DATA 16	94					
J24	MEM DATA 18	95					
J25	MEM DATA 20	96	6.0	0.0	0.5	V	1-4

NOTES:

1. Output voltage, low level, test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	4.5 V	± 45 mV	J1-J25
Power supply current limit	1.41 A	NA	J1-J25
Forcing current, (Iol)	6.0 mA	± 600 uA	J1-J25
Pattern voltage high, (VH) low, (VL)	3.0 V 0.0 V	± 100 mV ± 100 mV	J1-J25 J1-J25
Output voltage measurement	NA	± 25 mV	J1-J25

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

NOTES: - Continued.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing current shall be applied to the pin specified in the appropriate test conditions in table X and the voltage then measured.

3. The load shall be as indicated on figure 9.

4. Abbreviations used are defined in 6.1.

TABLE XI. Output leakage current, high and low level, test.

Test cond	Signal name	Pin no.	Forcing voltage (V)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
High level							
K1	DYNAMIC RAM	27	2.4	-0.05	0.05	mA	1-3
K2	PERFORMANCE0	72					
K3	HERE	84	2.4	-0.05	0.05	mA	1-3
Low level							
K4	DYNAMIC RAM	27	0.4	-0.05	0.05	mA	1-3
K5	PERFORMANCE0	72					
K6	HERE	84	0.4	-0.05	0.05	mA	1-3

NOTES:

1. Output leakage current, high and low level, test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	K1-K6
Power supply current limit	1.41 A	NA	K1-K6
Forcing voltage, (Voh) (Vol)	 2.4 V 0.4 V	 ± 50 mV ± 50 mV	 K1-K3 K4-K6
Pattern voltage high, (VH) low, (VL)	 3.0 V 0.0 V	 ± 100 mV ± 100 mV	 K1-K6 K1-K6
Output current measurement	NA	± 5 uA	K1-K6

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test to achieve the required state and make the indicated measurement at the appropriate pattern line.

NOTES: - Continued.

(c) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(d) The forcing voltage shall be applied to the pin specified in the appropriate test conditions in table XI and the current then measured. The forcing voltage overshoot shall not exceed 100 mV.

3. Abbreviations used are defined in 6.1.

TABLE XII. Input clamp diode voltage test.

Test cond	Signal name	Pin no.	Iin (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
L1	MEM ADRS A 0	2	-18.0	-1.2	0.0	V	1-3
L2	MEM ADRS A 1	3					
L3	MEM ADRS A 2	4					
L4	MEM ADRS A 3	5					
L5	MEM DATA 1	6					
L6	MEM DATA 3	7					
L7	MEM DATA 5	8					
L8	MEM DATA 7	9					
L9	MEM ADRS A 4	11					
L10	MEM ADRS A 5	12					
L11	MEM ADRS A 6	13					
L12	MEM ADRS A 7	14					
L13	MEM DATA 9	17					
L14	MEM DATA 11	18					
L15	MEM DATA 13	19					
L16	MEM DATA 15	20					
L17	WRITE DATA	22					
L18	WR CHK BIT	23					
L19	ENABLE CAS	24					
L20	ARRAY SEL X	26					
L21	MEM ADRS B 0	39	-18.0	-1.2	0.0	V	1-3

TABLE XII. Input clamp diode voltage test - Continued.

Test cond	Signal name	Pin no.	Vin (V)	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
L22	MEM ADRS B 1	41	-18.0	-1.2	0.0	V	1-3
L23	MEM ADRS B 2	42					
L24	MEM ADRS B 3	43					
L25	MEM DATA 17	44					
L26	MEM DATA 19	45					
L27	MEM DATA 21	46					
L28	MEM ADRS B 4	47					
L29	MEM ADRS B 5	48					
L30	MEM ADRS B 6	49					
L31	MEM ADRS B 7	50					
L32	MEM ADRS A 8	52					
L33	MEM ADRS A 9	53					
L34	MEM ADRS A10	54					
L35	MEM ADRS A11	55					
L36	MEM DATA 0	56					
L37	MEM DATA 2	57					
L38	MEM DATA 4	58					
L39	MEM DATA 6	59					
L40	MEM ADRS A12	61					
L41	MEM ADRS A13	62					
L42	MEM ADRS A14	63	-18.0	-1.2	0.0	V	1-3

TABLE XII. Input clamp diode voltage test - Continued.

Test cond	Signal name	Pin no.	Vin (V)	25 ± 5°C Initial limits Min	Max	Units	Notes
L43	MEM ADRS A15	64	-18.0	-1.2	0.0	V	1-3
L44	MEM DATA 8	67					
L45	MEM DATA 10	68					
L46	MEM DATA 12	69					
L47	MEM DATA 14	70					
L48	READ ENABLE	71					
L49	ARRAY SEL Y	76					
L50	MEM ADRS B 8	89					
L51	MEM ADRS B 9	91					
L52	MEM ADRS B10	92					
L53	MEM ADRS B11	93					
L54	MEM DATA 16	94					
L55	MEM DATA 18	95					
L56	MEM DATA 20	96					
L57	MEM ADRS B12	97					
L58	MEM ADRS B13	98					
L59	MEM ADRS B14	99					
L60	MEM ADRS B15	100	-18.0	-1.2	0.0	V	1-3

NOTES:

1. Input clamp diode voltage test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	Off	NA	L1-L60
Power supply current limit	NA	NA	L1-L60
Forcing current, (Iin)	-18 mA	± 1.8 mA	L1-L60
Pattern voltage high, (VH) low, (VL)	 NA NA	 NA NA	 L1-L60 L1-L60
Input voltage measurement	NA	± 60 mV	L1-L60

2. The following procedure is required to perform this test:

(a) No power shall be applied to the module.

(b) When making the test indicated on a pin, insure that the pin is disconnected from any drivers or comparators except those called for in the test.

(c) The forcing current shall be applied to the pin specified in the appropriate test conditions in table XII and the voltage then measured.

3. Abbreviations used are defined in 6.1.

TABLE XIII. Power supply filter capacitance test.

Test cond	Parameter	Pin numbers	25 ± 5°C Initial limits Min	Max	Units	Notes
M	PSFC	1	6.7	12.5	uF	1-4

NOTES:

1. Power supply filter capacitance test tolerance table.

Condition	Value	Accuracy	Test condition
Capacitance bridge frequency	1 KHz	± 100 Hz	M
Capacitance bridge voltage	0.3 Vp	± 30 mVp	M
Capacitance measurement	NA	± 290 nF	M

2. The capacitance bridge used in this test shall be item C01. The negative terminal shall be connected to the module ground and the positive terminal to the pin indicated in table XIII.

3. The test circuit shall be as indicated on figure 10.

4. Abbreviations used are defined in 6.1.

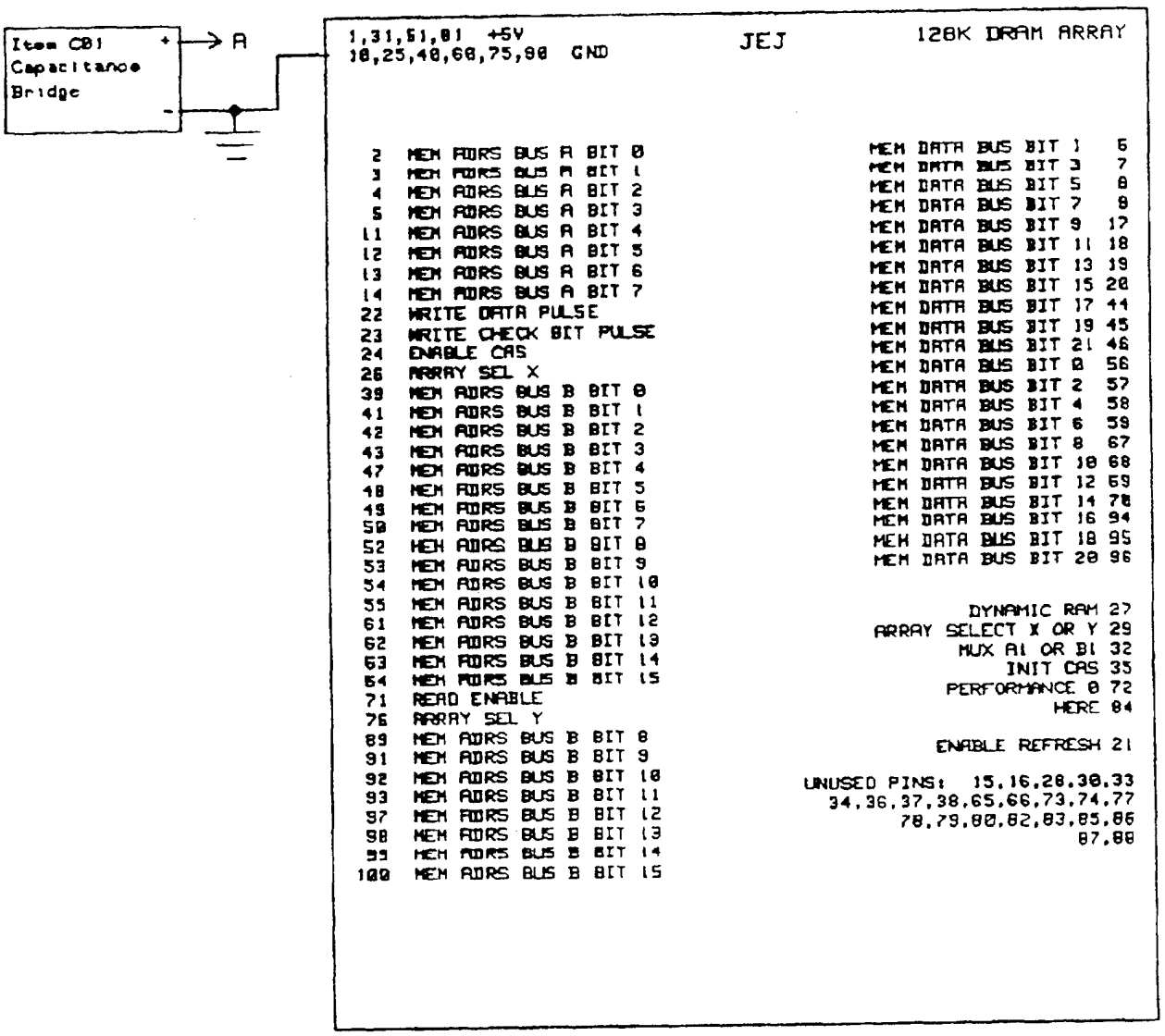


FIGURE 10. Power supply filter capacitance test circuit for table XIII.

TABLE XIV. Power supply current test.

Test cond	Parameter	Pin no.	25 ± 5°C Initial limits Min	Max	Units	Notes
N	Icc	1,31 51,81	350	1210	mA	1-3

NOTES:

1. Power supply current test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.5 V	± 55 mV	N
Power supply current limit	1.41 A	NA	N
Pattern voltage high, (VH)	3.0 V	± 100 mV	N
low, (VL)	0.0 V	± 100 mV	N
Power supply current measurement	NA	± 43 mA	N

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Precondition the module under test and take a measurement at the pattern line with the maximum power supply current as indicated in table XIV.

3. Abbreviations used are defined in 6.1.

TABLE XV. Functional test.

Test cond	Test description	Notes
P1	Functional test minimum power supply voltage maximum pattern rate (225 nS)	1-3
P2	Functional test maximum power supply voltage maximum pattern rate (225 nS)	1-3

NOTES:

1. Functional test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	4.5 V 5.5 V	± 45 mV ± 55 mV	P1 P2
Power supply current limit	1.41 A	NA	P1,P2
Pattern voltage high, (VH) low, (VL)	 2.4 V 0.4 V	 ± 100 mV ± 100 mV	 P1,P2 P1,P2
Output voltage verification high, (Voh) high, (Voh) low, (Vol)	 NA NA NA	 ± 105 mV ± 155 mV ± 20 mV	 P1 P2 P1,P2

NOTES: - Continued.

2. The following procedure is required to perform this test:

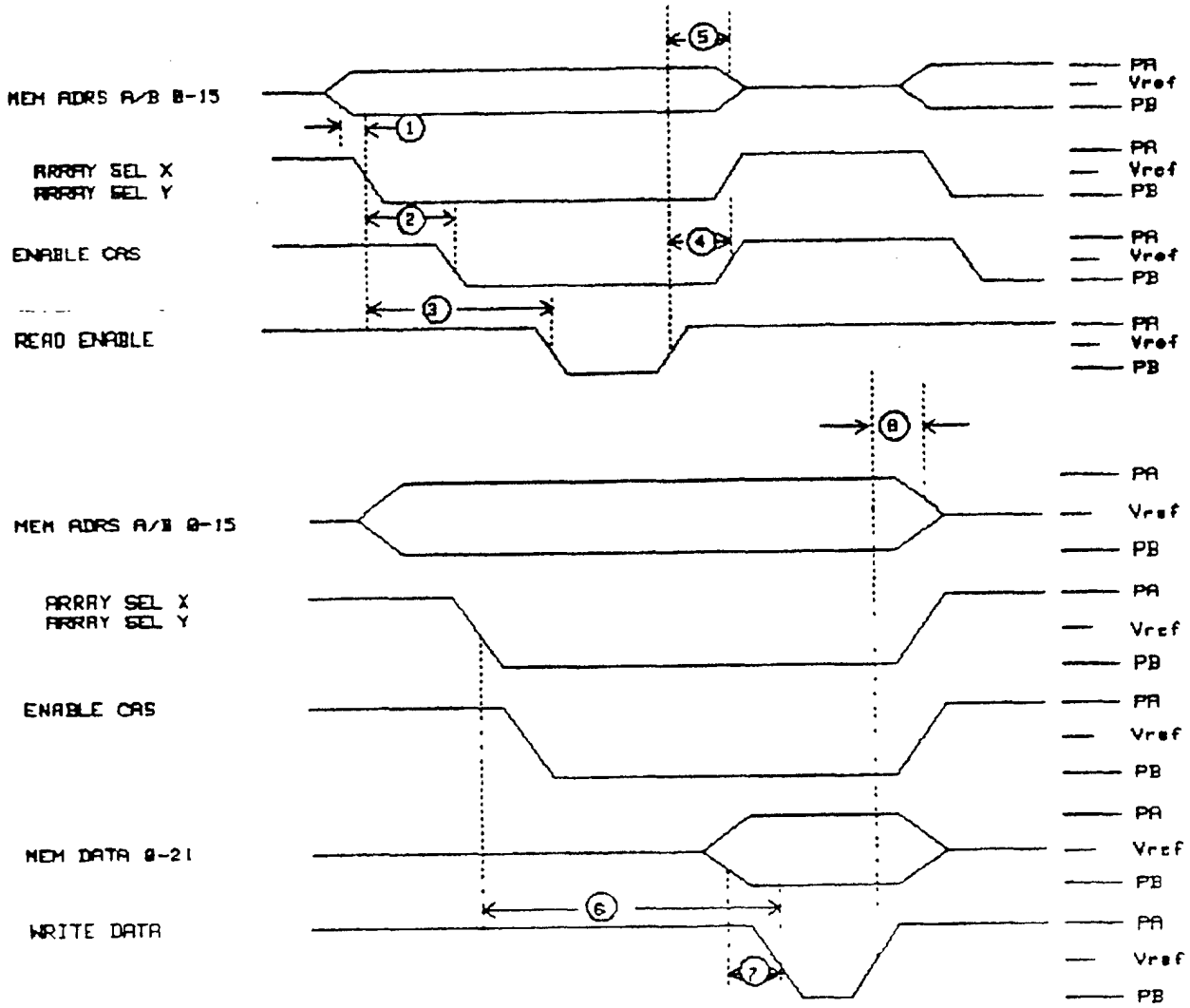
(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

(b) Use the appropriate pattern to verify the functional performance of the module as indicated in table XV using only a capacitive load of 100 pF (see figure 9). The output compare levels shall be as follows:

High level: $2.4\ V \leq Voh \leq Vcc$
Low level: $0.0\ V \leq Vol \leq 0.5\ V$

(c) The module inputs shall not violate the minimum input timing parameters referenced on figure 11.

3. Abbreviations used are defined in 6.1.



NOTES:

1. (1) MEM ADRS A/B 0-15 to ARRAY SEL X/ARRAY SEL Y.

   Setup time: 10 nS minimum.

2. (2) ARRAY SEL X/ARRAY SEL Y to ENABLE CAS.

   Setup time: 27 nS minimum.

FIGURE 11. Input timing parameters for table XV.

NOTES: - Continued.

3. (3) ARRAY SEL X/ARRAY SEL Y to READ ENABLE.

   Setup time: 85 nS minimum.

4. (4) READ ENABLE to ENABLE CAS.

   Setup time: 1 nS minimum.

5. (5) READ ENABLE to MEM ADRS A/B 0-15.

   Setup time: 0 nS minimum.

6. (6) ARRAY SEL X/ARRAY SEL Y to WRITE DATA.

   Setup time: 83 nS minimum.

7. (7) MEM DATA 0-21 to WRITE DATA.

   Setup time: 9 nS minimum.

8. (8) WRITE DATA to MEM ADRS A/B 0-15.

   Setup time: 8 nS minimum.

FIGURE 11. Input timing parameters for table XV - Continued.

TABLE XVI. Dynamic test.

Test cond	Test description	Notes
Q1	Dynamic test, sample maximum pattern rate (225 nS) minimum power supply	1-6
Q2	Dynamic test, sample maximum pattern rate (225 nS) maximum power supply	1-6
Q3	Dynamic test, qualification maximum pattern rate (225 nS) minimum power supply	1-6
Q4	Dynamic test, qualification maximum pattern rate (225 nS) maximum power supply	1-6

NOTES:

1. Dynamic test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	4.5 V 5.5 V	± 45 mV ± 55 mV	Q1,Q3 Q2,Q4
Power supply current limit	1.41 A	NA	Q1-Q4
Input voltage high, (VH) low, (VL)	 2.4 V 0.4 V	 ± 100 mV ± 100 mV	 Q1-Q4 Q1-Q4

NOTES: - Continued.

Condition	Value	Accuracy	Test condition
Output voltage verification			
high, (Voh)	NA	± 100 mV	Q1,Q3
high, (Voh)	NA	± 100 mV	Q2,Q4
low, (Vol)	NA	± 100 mV	Q1-Q4

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

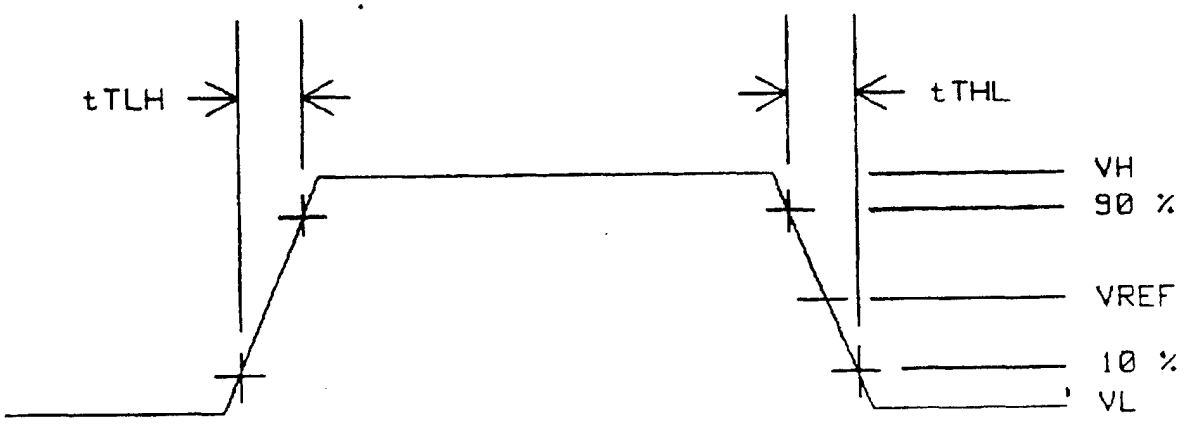
(b) The output compare levels shall be as follows:

High level: $Vref \leq Voh \leq Vcc$
Low level: $0.0\ V \leq Vol \leq Vref$

(c) The dynamic parameters are found in table XVII.

3. The load circuit for this test is specified on figure 9.

4. Input/Output (I/O) waveforms are as referenced on figure 12. All of the input waveforms shall have the following characteristics:



NOTES: - Continued.

Where:

(a) VH and VL are as specified in the test tolerance table.

(b) tTLH = tTHL $\leq$ 10 nS.

(c) Vref = 1.6 V.

5. This test shall be performed as indicated in table XVI.

6. Abbreviations used are defined in 6.1.

TABLE XVII. Dynamic parameters.

Ref num	Sym	Parameter	Minimum limit			Maximum limit			Unit	Figs
			-55°C	25°C	85°C	-55°C	25°C	85°C		
1	tsu	MEM ADRS A 0-15 to ARRAY SEL X	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS A 0-15 to ARRAY SEL Y	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS B 0-15 to ARRAY SEL X	10	10	10	-	-	-	nS	12
1	tsu	MEM ADRS B 0-15 to ARRAY SEL Y	10	10	10	-	-	-	nS	12
2	tsu	ARRAY SEL X to ENABLE CAS	27	27	27	-	-	-	nS	12
2	tsu	ARRAY SEL Y to ENABLE CAS	27	27	27	-	-	-	nS	12
3	tsu	ARRAY SEL X to READ ENABLE	85	85	85	-	-	-	nS	12
3	tsu	ARRAY SEL Y to READ ENABLE	85	85	85	-	-	-	nS	12
4	tpd	ARRAY SEL X to MEM DATA 0-21	-	-	-	180	180	180	nS	12
4	tpd	ARRAY SEL Y to MEM DATA 0-21	-	-	-	180	180	180	nS	12

TABLE XVII. Dynamic parameters - Continued.

Ref num	Sym	Parameter	Minimum limit			Maximum limit			Unit	Figs
			-55°C	25°C	85°C	-55°C	25°C	85°C		
5	tsu	READ ENABLE to ENABLE CAS	1	1	1	-	-	-	nS	12
6	tsu	READ ENABLE to MEM ADRS A 0-15	0	0	0	-	-	-	nS	12
6	tsu	READ ENABLE to MEM ADRS B 0-15	0	0	0	-	-	-	nS	12
7	tpw	ARRAY SEL X	156	156	156	-	-	-	nS	12
7	tpw	ARRAY SEL Y	156	156	156	-	-	-	nS	12
8	tsu	ARRAY SEL X to WRITE DATA	83	83	83	-	-	-	nS	12
8	tsu	ARRAY SEL Y to WRITE DATA	83	83	83	-	-	-	nS	12
9	tsu	MEM DATA 0-21 to WRITE DATA	9	9	9	-	-	-	nS	12
10	tpw	WRITE DATA	50	50	50	-	-	-	nS	12
11	tsu	WRITE DATA to MEM ADRS A 0-15	8	8	8	-	-	-	nS	12
11	tsu	WRITE DATA to MEM ADRS B 0-15	8	8	8	-	-	-	nS	12

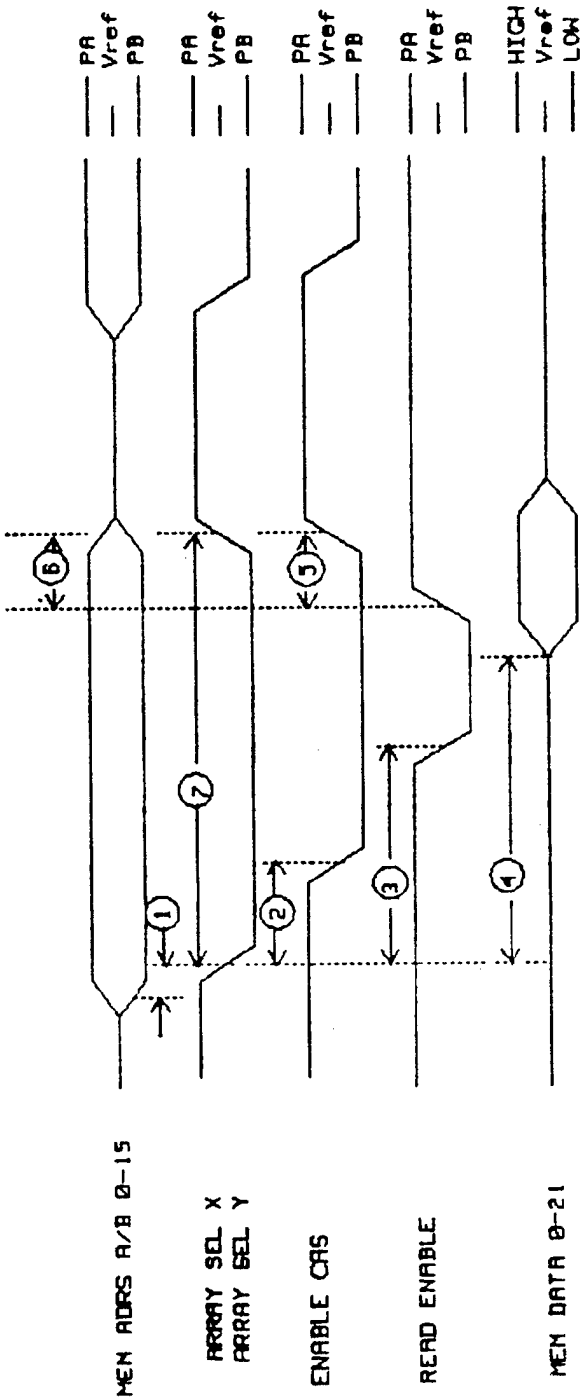


FIGURE 12a. Dynamic waveforms for table XVII.

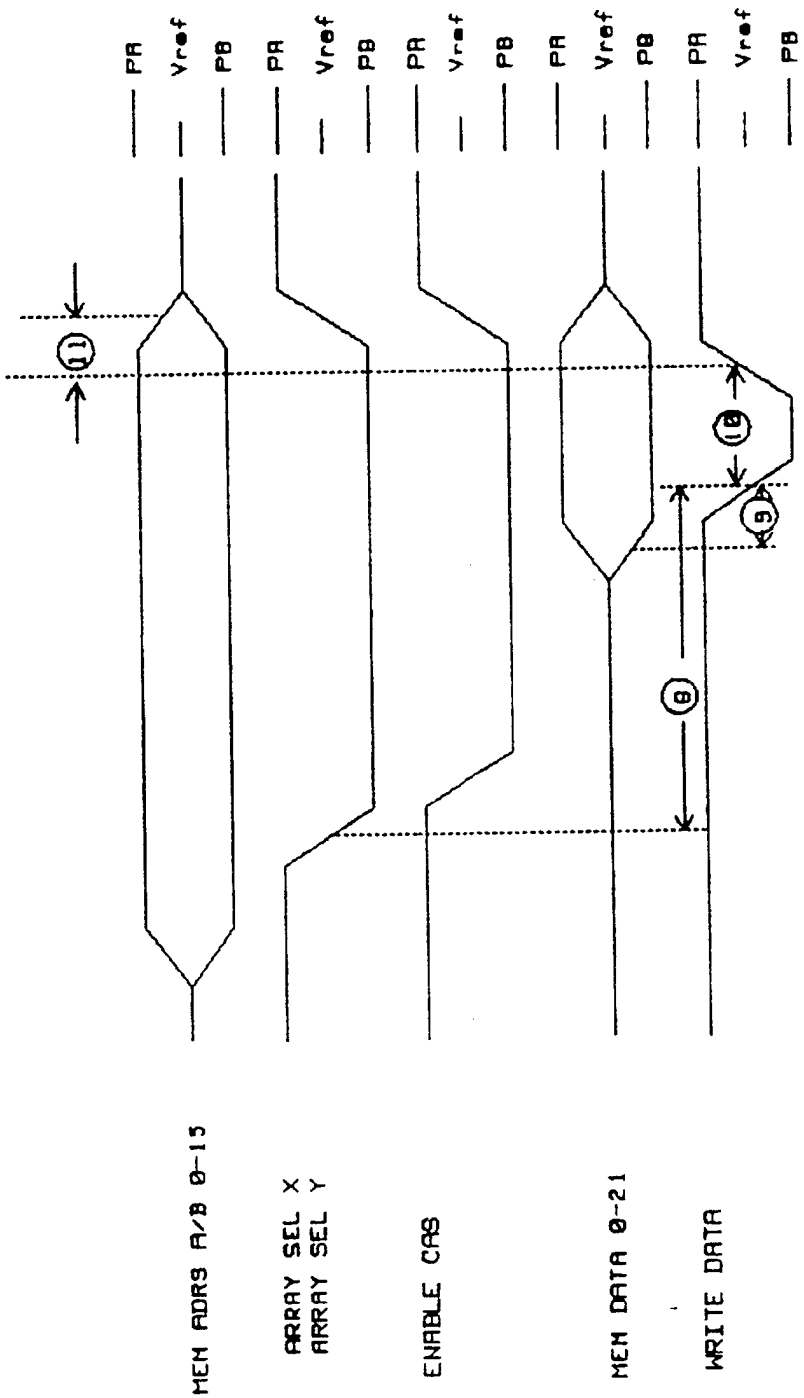


FIGURE 12b. Dynamic waveforms for table XVII.

TABLE XVIII. Input and output capacitance test.

Test cond	Signal name	Pin no.	25 ± 5°C Initial limits Min	Max	Units	Notes
Inputs						
R1	MEM ADRS A 0	2	4	75	pF	1-4
R2	MEM ADRS A 1	3				
R3	MEM ADRS A 2	4				
R4	MEM ADRS A 3	5				
R5	MEM ADRS A 4	11				
R6	MEM ADRS A 5	12				
R7	MEM ADRS A 6	13				
R8	MEM ADRS A 7	14	4	75	pF	1-4
R9	WRITE DATA	22	8	100	pF	1-4
R10	WR CHK BIT	23	4	75	pF	1-4
R11	ENABLE CAS	24	10	125	pF	1-4
R12	ARRAY SEL X	26	10	100	pF	1-4
R13	MEM ADRS B 0	39	4	75	pF	1-4
R14	MEM ADRS B 1	41				
R15	MEM ADRS B 2	42				
R16	MEM ADRS B 3	43				
R17	MEM ADRS B 4	47				
R18	MEM ADRS B 5	48	4	75	pF	1-4
R19	MEM ADRS B 6	49	4	100	pF	1-4
R20	MEM ADRS B 7	50	4	100	pF	1-4

TABLE XVIII. Input and output capacitance test - Continued.

Test cond	Signal name	Pin no.	25 ± 5°C Initial limits Min	Max	Units	Notes
R21	MEM ADRS A 8	52	2	75	pF	1-4
R22	MEM ADRS A 9	53				
R23	MEM ADRS A10	54				
R24	MEM ADRS A11	55				
R25	MEM ADRS A12	61				
R26	MEM ADRS A13	62				
R27	MEM ADRS A14	63				
R28	MEM ADRS A15	64	2	75	pF	1-4
R29	READ ENABLE	71	6	175	pF	1-4
R30	ARRAY SEL Y	76	10	100	pF	1-4
R31	MEM ADRS B 8	89	2	75	pF	1-4
R32	MEM ADRS B 9	91				
R33	MEM ADRS B10	92				
R34	MEM ADRS B11	93	2	75	pF	1-4
R35	MEM ADRS B12	97	2	100	pF	1-4
R36	MEM ADRS B13	98	2	75	pF	1-4
R37	MEM ADRS B14	99	2	75	pF	1-4
R38	MEM ADRS B15	100	2	100	pF	1-4
	Bidirectionals					
R39	MEM DATA 1	6	4	75	pF	1-4
R40	MEM DATA 3	7	4	75	pF	1-4

TABLE XVIII. Input and output capacitance test - Continued.

Test cond	Signal name	Pin no.	25 ± 5°C Initial limits Min	25 ± 5°C Initial limits Max	Units	Notes
R41	MEM DATA 5	8	4	75	pF	1-4
R42	MEM DATA 7	9				
R43	MEM DATA 9	17				
R44	MEM DATA 11	18				
R45	MEM DATA 13	19				
R46	MEM DATA 15	20				
R47	MEM DATA 17	44				
R48	MEM DATA 19	45				
R49	MEM DATA 21	46				
R50	MEM DATA 0	56				
R51	MEM DATA 2	57				
R52	MEM DATA 4	58				
R53	MEM DATA 6	59				
R54	MEM DATA 8	67				
R55	MEM DATA 10	68				
R56	MEM DATA 12	69				
R57	MEM DATA 14	70				
R58	MEM DATA 16	94				
R59	MEM DATA 18	95				
R60	MEM DATA 20	96	4	75	pF	1-4

NOTES:

1. Input and output capacitance test tolerance table.

Condition	Value	Accuracy	Test condition
Capacitance meter frequency	1 MHz	± 100 KHz	R1-R60
Capacitance meter voltage	15 mV	± 1.5 mV	R1-R60
Capacitance measurement	NA	± 3.55 pF	R1-R8
	NA	± 4.6 pF	R9
	NA	± 3.55 pF	R10
	NA	± 5.75 pF	R11
	NA	± 4.5 pF	R12
	NA	± 3.55 pF	R13-R18
	NA	± 4.8 pF	R19,R20
	NA	± 3.65 pF	R21-R28
	NA	± 8.45 pF	R29
	NA	± 4.5 pF	R30
	NA	± 3.65 pF	R31-R34
	NA	± 4.9 pF	R35
	NA	± 3.65 pF	R36,R37
	NA	± 4.9 pF	R38
	NA	± 3.55 pF	R39-R60

2. The capacitance meter used in this test shall be item C05. The negative terminal shall be connected to the module ground and the positive terminal to the pin indicated in table XVIII.

3. The test circuit shall be as indicated on figure 13.

4. Abbreviations used are defined in 6.1.

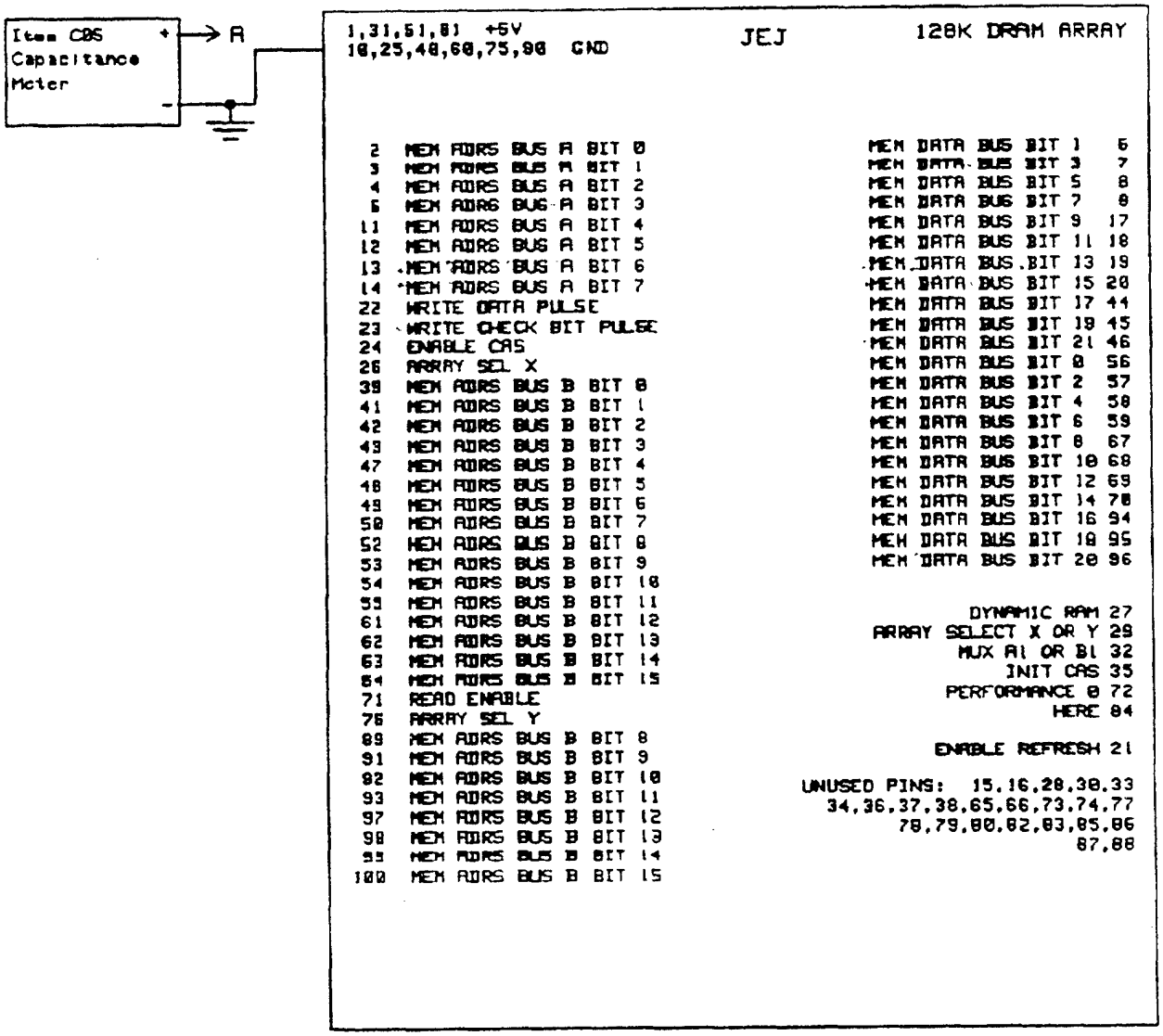


FIGURE 13. Input and output capacitance test circuit for table XVIII.

TABLE XIX. Power supply transient amplitude test.

Test cond	Parameter	Pin no.	25 ± 5°C Initial limits Min	Max	Units	Notes
T	PSTA	1	0	400	mV	1-4

NOTES:

1. Power supply transient amplitude test tolerance table.

Condition	Value	Accuracy	Test condition
Power supply, (Vcc)	5.0 V	± 250 mV	T
Power supply current limit	1.41 A	NA	T
Pattern voltage high, (VH) low, (VL)	3.0 V 0.0 V	± 100 mV ± 100 mV	T T
Power supply transient amplitude measurement	NA	± 20 mV	T

2. The following procedure is required to perform this test:

(a) The module power supply and ground pins shall be connected as specified in the power supply stress test table to an external source. The power supply voltage, including overshoot, shall not exceed the value specified in the power supply stress test tolerance table.

NOTES: - Continued.

(b) Precondition the module under test and make the indicated measurement for the test condition shown in table XIX.

(c) Vcc pins 1 and 31 shall be shorted together, pins 51 and 81 shall be shorted together and the scope point, probe 'A', shall be connected to the pin indicated in table XIX.

(d) Using the oscilloscope, D06, inspect for the most negative spike as shown on figure 14 at the pattern line with the maximum power supply current.

(e) The maximum probe capacitance is 15 pF. There shall be no other capacitance present on Vcc to ground.

3. The test circuit shall be as indicated on figure 15.

4. Abbreviations used are defined in 6.1.

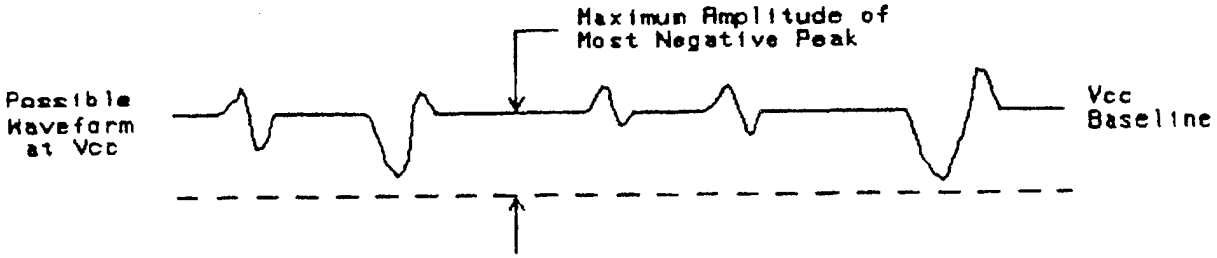
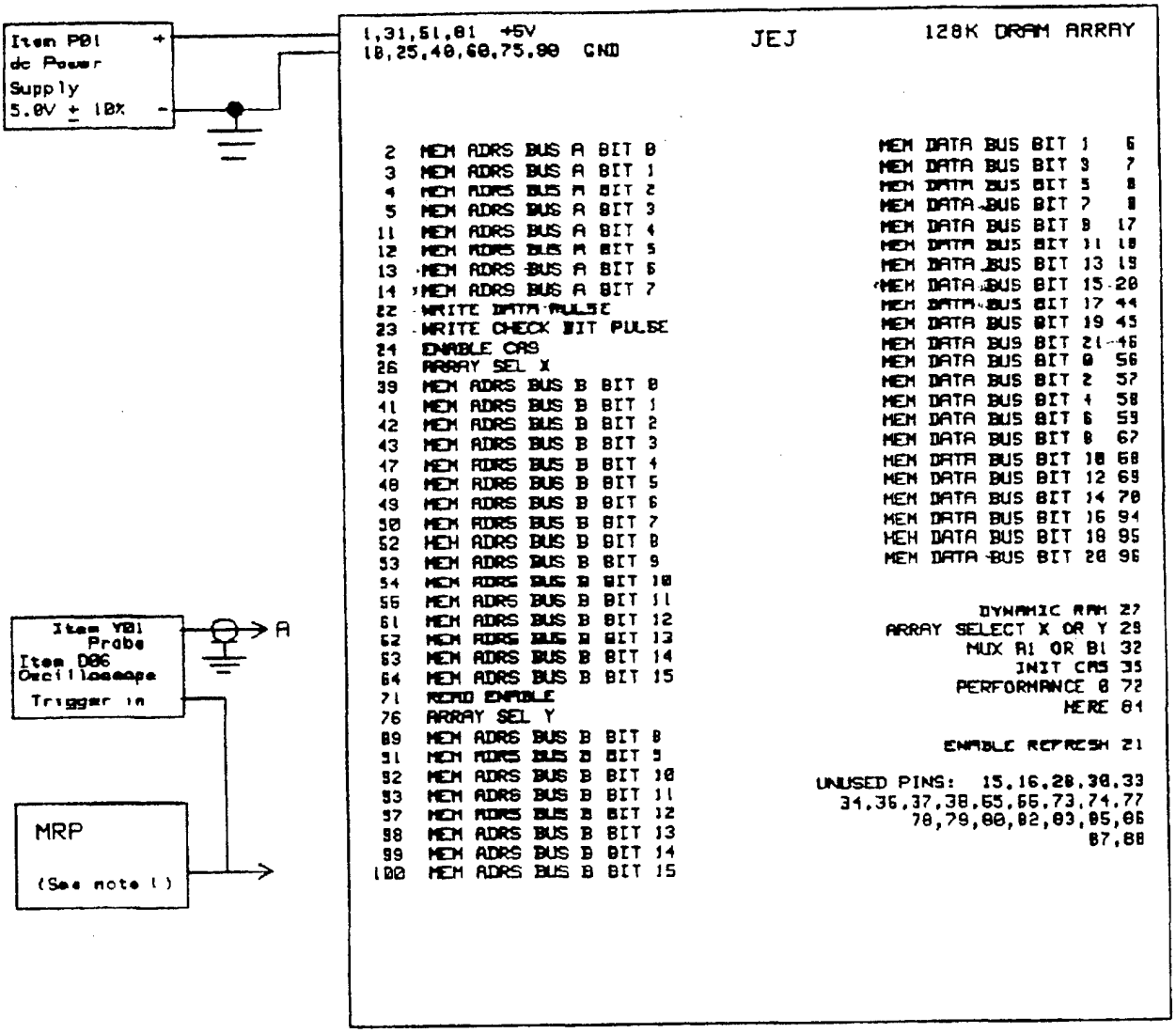


FIGURE 14. Power supply transient amplitude waveform for table XIX.



NOTE:

1. MRP or emulator capable of reproducing system backpanel characteristics.

FIGURE 15. Power supply transient amplitude test circuit for table XIX.

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	MIL-M-28787/432	

3. DOCUMENT TITLE

Modules, Standard Electronic, Memory Array, 128K Dynamic Random Access Module, Key Code JEJ

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

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INCH-POUND

MIL-M-28787/432
NOTICE 1
20 April 1998

MILITARY SPECIFICATION

MODULES, STANDARD ELECTRONIC MEMORY ARRAY, 128K DYNAMIC RANDOM ACCESS MODULE KEY CODE JEJ

MIL-M-28787/432, including Amendment 1, dated 29 September 1993, is inactive for new design and is no longer used, except for replacement purposes.

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